MODEL 41-3A
CENTRAL OFFICE SERVICE ANALYZER

SERVICE MANUAL

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Northeast Electronics Instruction Manual
A0041-13-603 Issue 1 February 1980

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679 810

Northeast Electronics Instruction Manual
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TABLE OF CONTENTS

SECTION	TITLE	PAGE
1	INTRODUCTION	1–1
2	DIAGRAMS	2–1
3	ELECTRONIC PARTS LISTS	3–1
4	PERFORMANCE SPECIFICATIONS	4–1

LIST OF ILLUSTRATIONS

FIGURE	TITLE	PAGE
2–1	TTS 41-3A Overall Block Diagram	2–3
2–2	Tip/Ring Path Diagram	2–4
2–3	Dialing Function Diagram	2–5
2–4	Measure Function Diagram	2–6
2–5	Display Function Diagram	2–7
2–6	Timing Function Diagram	2–8
2–7	Processing Function Diagram	2–9
2–8	Teleprinter Function Diagram	2–10
2–9	Software Structure Diagram	2–11
2–10	Line Switching Interface Component Location Diagram	2–12
2–11	Line Switching Interface Schematic Diagram	2–13
2–12	Dialing/Hold Component Location Diagram	2–14
2–13	L1/Control Board Component Location Diagram	2–14
2–14	Dialing/Hold Schematic Diagram	2–15
2–15	Digital TT/MF Generator Component Location Diagram	2–16
2–16	Digital TT/MF Generator Schematic Diagram	2–17
2–17	Monitor Tones Detector Component Location Diagram	2–19
2–18	Monitor Tones Detector Schematic Diagram (Sheet 1 of 2)	2–20
2–18	Monitor Tones Detector Schematic Diagram (Sheet 2 of 2)	2–21
2–19	Dial Control/Timer Component Location Diagram	2–23
2–20	Dial Control/Timer Schematic Diagram (Sheet 1 of 2)	2–24
2–20	Dial Control/Timer Schematic Diagram (Sheet 2 of 2)	2–25
2–21	System I/O Board Component Location Diagram	2–27
2–22	System I/O Board Schematic Diagram (Sheet 1 of 2)	2–28
2–22	System I/O Board Schematic Diagram (Sheet 2 of 2)	2–29
2–23	Display I/O Board Component Location Diagram	2–31
2–24	Display I/O Board Schematic Diagram (Sheet 1 of 2)	2–32
2–24	Display I/O Board Schematic Diagram (Sheet 2 of 2)	2–33
2–25	Processor Component Location Diagram	2–34
2–26	Processor Schematic Diagram	2–35
2–27	Memory Board Component Location Diagram	2–36
2–28	Memory Board Schematic Diagram	2–37
2–29	Optional TTY Interface Component Location Diagram	2–38
2–30	Optional TTY Interface Schematic Diagram	2–39
2–31	Null Modem Cable Schematic Diagram (Part Of TTY Option)	2–41
2–32	Mother Board Component Location Diagram	2–42
2–33	Sleeve Holding Circuit Component Location Diagram	2–42
2–34	Card Cage Assembly Schematic Diagram	2–43

LIST OF ILLUSTRATIONS

FIGURE	TITLE	PAGE
2–35	Front Panel Assembly Component Location Diagrams	2–45
2–36	Programmer I Component Location Diagram	2–46
2–37	Programmer II Component Location Diagram	2–46
2–38	Keyboard Component Location Diagram	2–46
2–39	Front Panel Schematic Diagram	2–47
2–40	Display Board Component Location Diagram	2–49
2–41	Display Board Schematic Diagram (Sheet 1 of 2)	2–50
2–41	Display Board Schematic Diagram (Sheet 2 of 2)	2–51
2–42	Line Control Module Component Location Diagram	2–53
2–43	Line Control Board Component Location Diagram	2–54
2–44	Loop And Leak Network Component Location Diagram	2–54
2–45	Line Control And Loop & Leak Schematic Diagram	2–55
2–46	Incoming Circuit Component Location Diagram	2–56
2–47	Incoming Circuit Schematic Diagram	2–57
2–48	MCS Module Component Location Diagram	2–58
2–49	MCS Module Schematic Diagram	2–59
2–50	Rear Panel Assembly Component Location Diagram	2–60
2–51	Power Wiring Schematic Diagram	2–61

LIST OF TABLES

TABLE	TITLE	PAGE
3 – 1	Overall Assembly Parts List	3–1
3 – 2	Line Switching Interface B0041-13-018 A1 Parts List	3–2
3 – 3	Dialing/Hold B0041-13-019 A2 Parts List	3–3
3 – 4	L1 Control B0041-13-072 A2A7 Parts List	3–4
3 – 5	Digital TT/MF Generator C0041-13-020 A4 Parts List	3–4
3 – 6	Monitor Tones Detector C0041-13-021 A5 Parts List	3–5
3 – 7	Dial Control/Timer C0041-13-022 A6 Parts List	3–7
3 – 8	System I/O Board C0041-13-023 A7 Parts List	3–8
3 – 9	Display I/O Board C0041-13-024 A8 Parts List	3–9
3–10	Processor B0001-01-078 A9 Parts List	3–10
3–11	Memory Board B0041-13-041 A10 Parts List	3–11
3–12	TTY Interface B0041-13-064 A11 Parts List	3–11
3–13	Card Cage Assembly D0041-13-047 A12 Parts List	3–12
3–14	Mother Board D0041-13-011 A12A1 Parts List	3–12
3–15	Sleeve Holding Circuit B0041-13-033 A12A2 Parts List	3–12
3–16	Front Panel Assembly D0041-13-045 A13 Parts List	3–12
3–17	Programmer I B0041-13-013 A13A1 Parts List	3–13
3–18	Programmer II B0041-13-012 A13A2 Parts List	3–13
3–19	Display Board D0041-13-010 A13A3 Parts List	3–13
3–20	Keyboard B0041-13-017 A13A4 Parts List	3–14
3–21	Low Level Switch Assembly B0041-13-029 A13A5 Parts List	3–14
3–22	EML Switch Assembly B0041-13-030 A13A6 Parts List	3–15
3–23	High Level Switch Assembly B0041-13-031 A13A7 Parts List	3–15
3–24	Line Control Module Assembly D0041-13-048 A13A8 Parts List	3–15
3–25	Line Control Board B0041-13-014 A13A8A1 Parts List	3–16
3–26	Loop/Leak Switch Assembly B0041-13-053 A13A8A2 Parts List	3–16
3–27	Rear Panel Assembly D0041-13-046 A14 Parts List	3–16
3–28	Incoming Circuit B0041-13-015 A14A1 Parts List	3–17
3–29	MCS Module D0041-13-049 A14A2 Parts List	3–18

SECTION 1

INTRODUCTION

1.1 This manual provides maintenance information for the TTS 41-3A Service Analyzer. Included are:

- ☐ Functional block diagrams (Section 2),
- ☐ Schematic diagrams (Section 2),
- ☐ Component location diagrams (Section 2),
- ☐ Parts lists (Section 3),
- ☐ Performance specifications for all electronic assemblies (Section 4).

1.2 Additional information pertaining to the 41-3A Service Analyzer is provided in other Instruction Manuals available from Northeast Electronics. These manuals are listed briefly below.

a. **A0041-13-600**. Contains general description, specifications, installation data, operating and application information.

b. **A0041-13-601**. Provides installation and operating information for the MF Option (A0041-13-901).

c. **A0041-13-602**. Gives installation and operating information for the Teleprinter Option (A0041-13-902).

SECTION 2

DIAGRAMS

2.1 This section contains diagrams which document the circuits within the Model TTS 41-3A Service Analyzer. Functional block diagrams are given first which show the interrelationships of the analyzer's electronic assemblies. The block diagrams are followed by detailed schematic diagrams for each assembly. Component location diagrams are also included to show the physical location of each electronic part.

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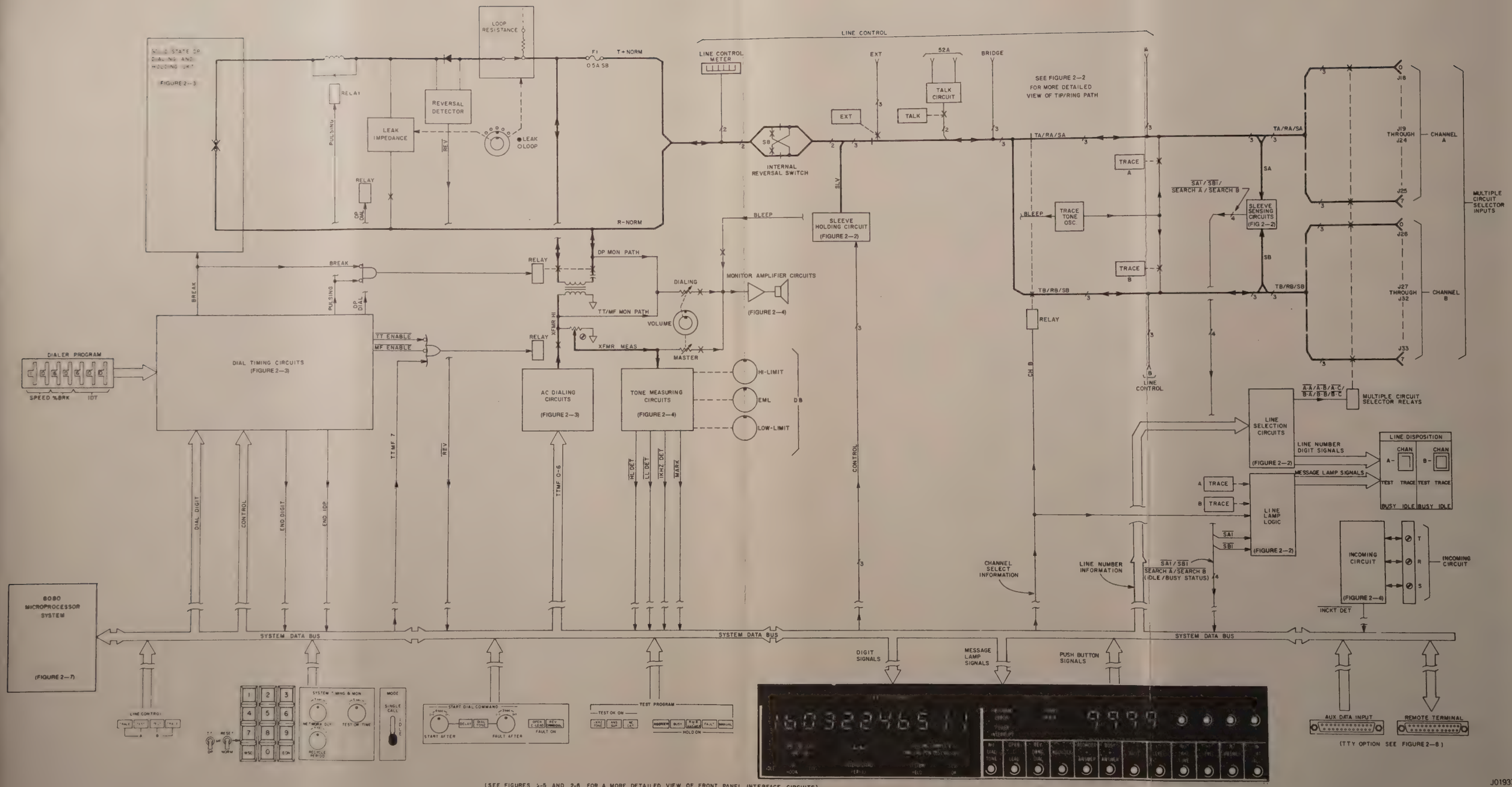


(SEE FIGURES 2-5 AND 2-6 FOR A MORE DETAILED VIEW OF FRONT PANEL INTERFACE CIRCUITS)

J01937

Figure 2—1. TTS 41-3A Overall Block Diagram.

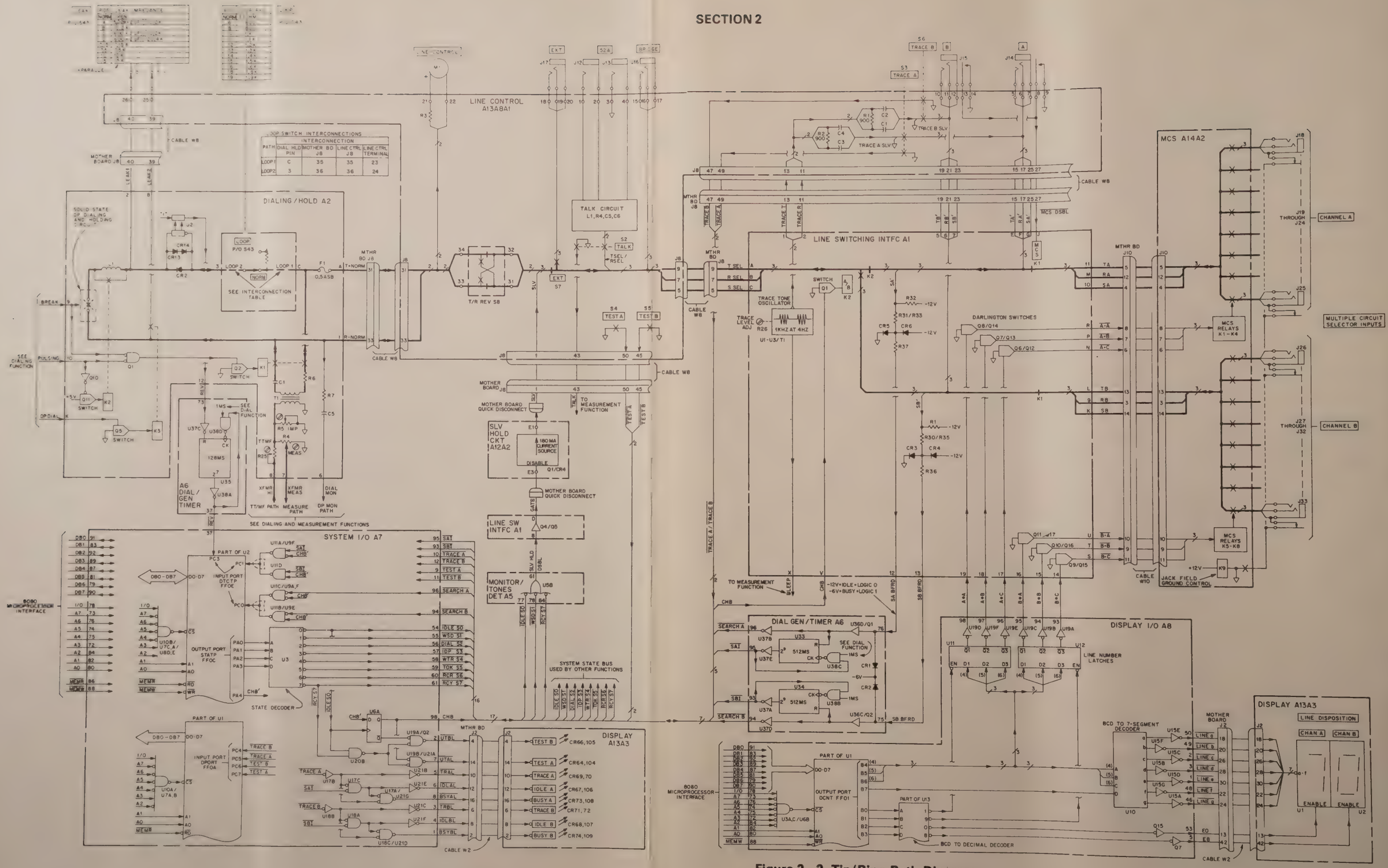
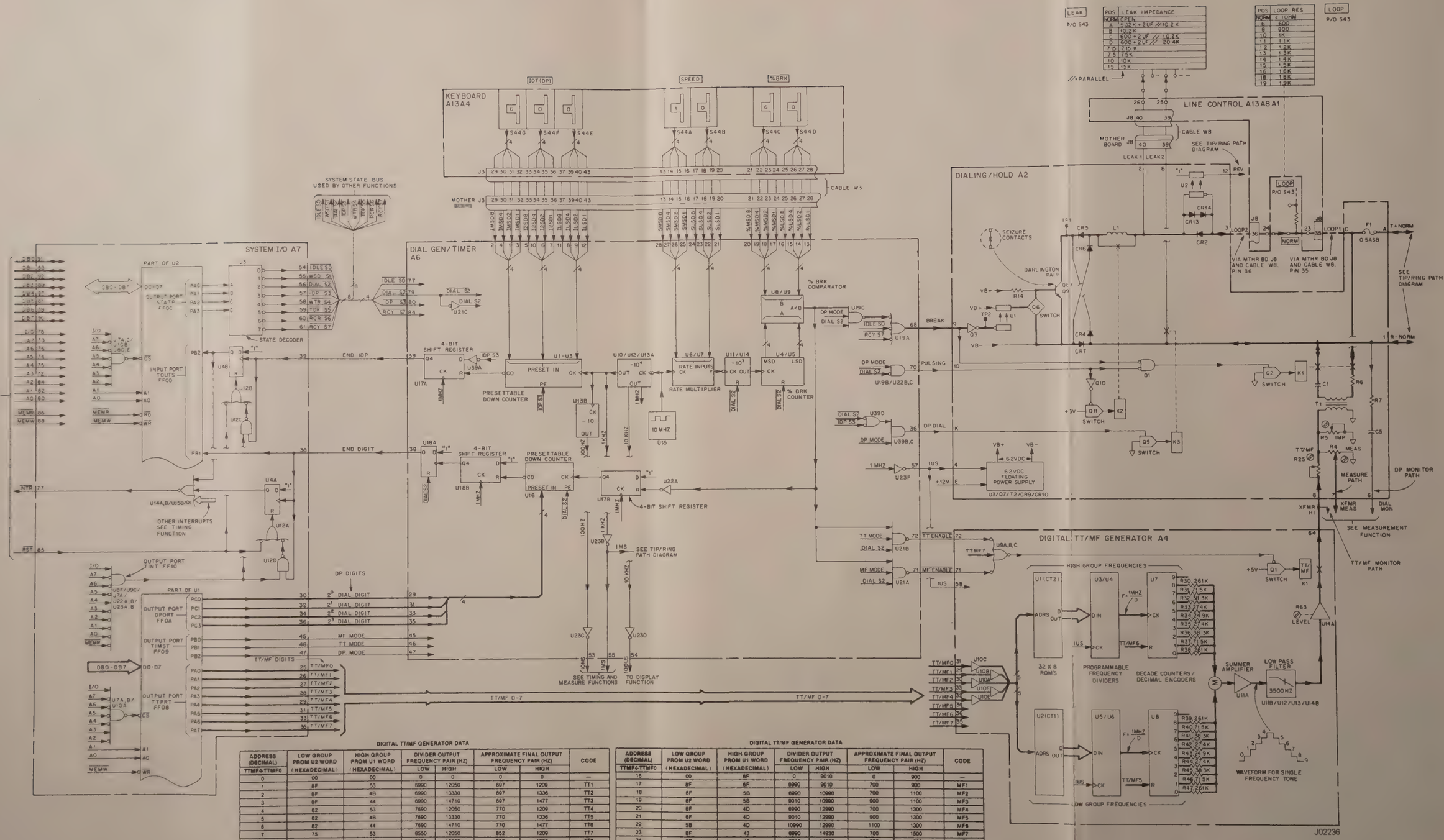


Figure 2—2. Tip/Ring Path Diagram.

J01951



DIGITAL TT/MF GENERATOR DATA

ADDRESS (DECIMAL) TTMF4-TTMF0	LOW GROUP PROM U2 WORD (HEXADECIMAL)	HIGH GROUP PROM U1 WORD (HEXADECIMAL)	DIVIDER OUTPUT FREQUENCY PAIR (HZ) LOW	DIVIDER OUTPUT FREQUENCY PAIR (HZ) HIGH	APPROXIMATE FINAL OUTPUT FREQUENCY PAIR (HZ) LOW	APPROXIMATE FINAL OUTPUT FREQUENCY PAIR (HZ) HIGH	CODE
0	00	00	0	0	0	0	—
1	8F	53	6990	12050	697	1209	TT1
2	8F	4B	6990	13330	697	1336	TT2
3	8F	44	6990	14710	697	1477	TT3
4	82	53	7690	12050	770	1209	TT4
5	82	4B	7690	13330	770	1336	TT5
6	82	44	7690	14710	770	1477	TT6
7	75	53	8550	12050	852	1209	TT7
8	75	4B	8550	13330	852	1336	TT8
9	75	44	8550	14710	852	1477	TT9
10	6A	4B	9430	13330	941	1336	TT0
11	6A	53	9430	12050	941	1209	TT *
12	6A	44	9430	14710	941	1477	TT#
13	00	00	0	0	0	0	—
14	00	2A	0	23810	0	2400	SF1
15	00	26	0	26320	0	2600	SF2

DIGITAL TT/MF GENERATOR DATA

ADDRESS (DECIMAL) TTMF4-TTMF0	LOW GROUP PROM U2 WORD (HEXADECIMAL)	HIGH GROUP PROM U1 WORD (HEXADECIMAL)	DIVIDER OUTPUT FREQUENCY PAIR (HZ) LOW	DIVIDER OUTPUT FREQUENCY PAIR (HZ) HIGH	APPROXIMATE FINAL OUTPUT FREQUENCY PAIR (HZ) LOW	APPROXIMATE FINAL OUTPUT FREQUENCY PAIR (HZ) HIGH	CODE
16	00	8F	0	9010	0	900	—
17	8F	6F	6990	9010	700	900	MF1
18	8F	5B	6990	10990	700	1100	MF2
19	6F	5B	9010	10990	900	1100	MF3
20	8F	4D	6990	12990	700	1300	MF4
21	6F	4D	9010	12990	900	1300	MF5
22	5B	4D	10990	12990	1100	1300	MF6
23	8F	43	6990	14930	700	1500	MF7
24	6F	43	9010	14930	900	1500	MF8
25	5B	43	10990	14930	1100	1500	MF9
26	4D	43	12990	14930	1300	1500	MF0
27	5B	3B	10990	16950	1100	1700	KP (KP1)
28	43	3B	14930	16950	1500	1700	ST
29	6F	3B	9990	16950	700	1700	ST3P (CD11)
30	6F	3B	9010	16950	900	1700	STP (CD12)
31	4D	3B	12990	16950	1300	1700	ST2P (KP2)

Figure 2—3. Dialing Function Diagram.

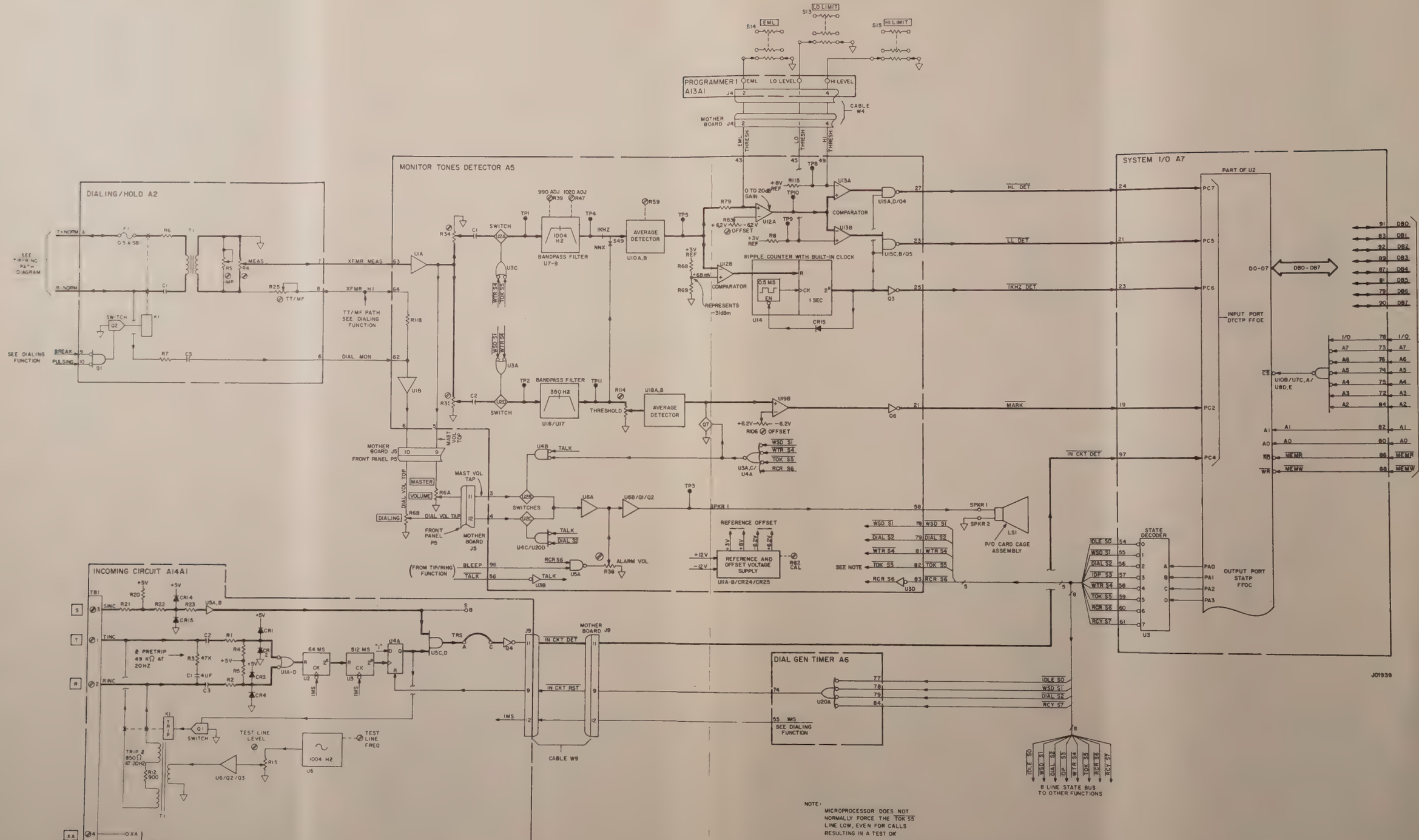


Figure 2—4. Measure Function Diagram.

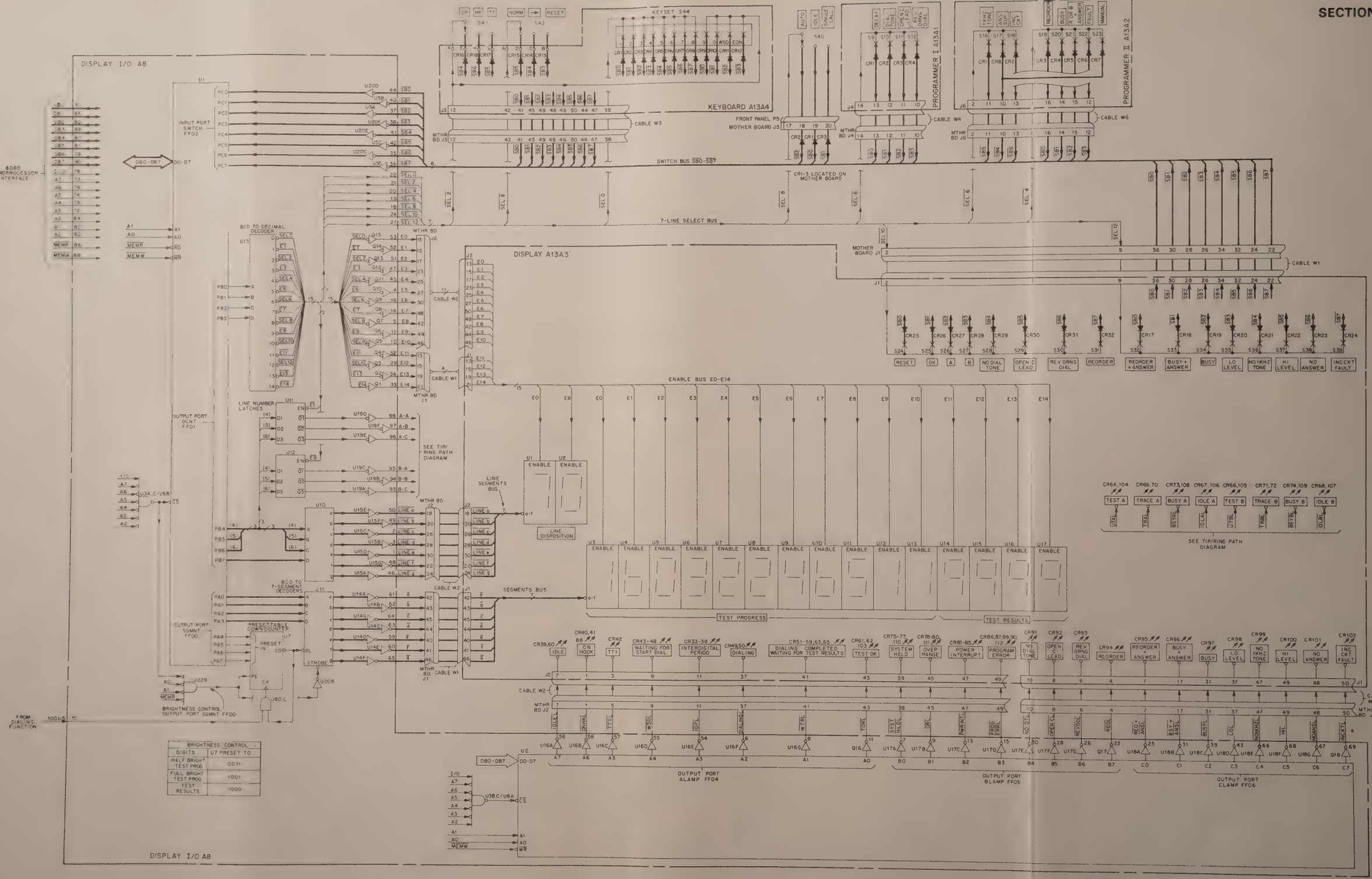


Figure 2—5. Display Function Diagram.

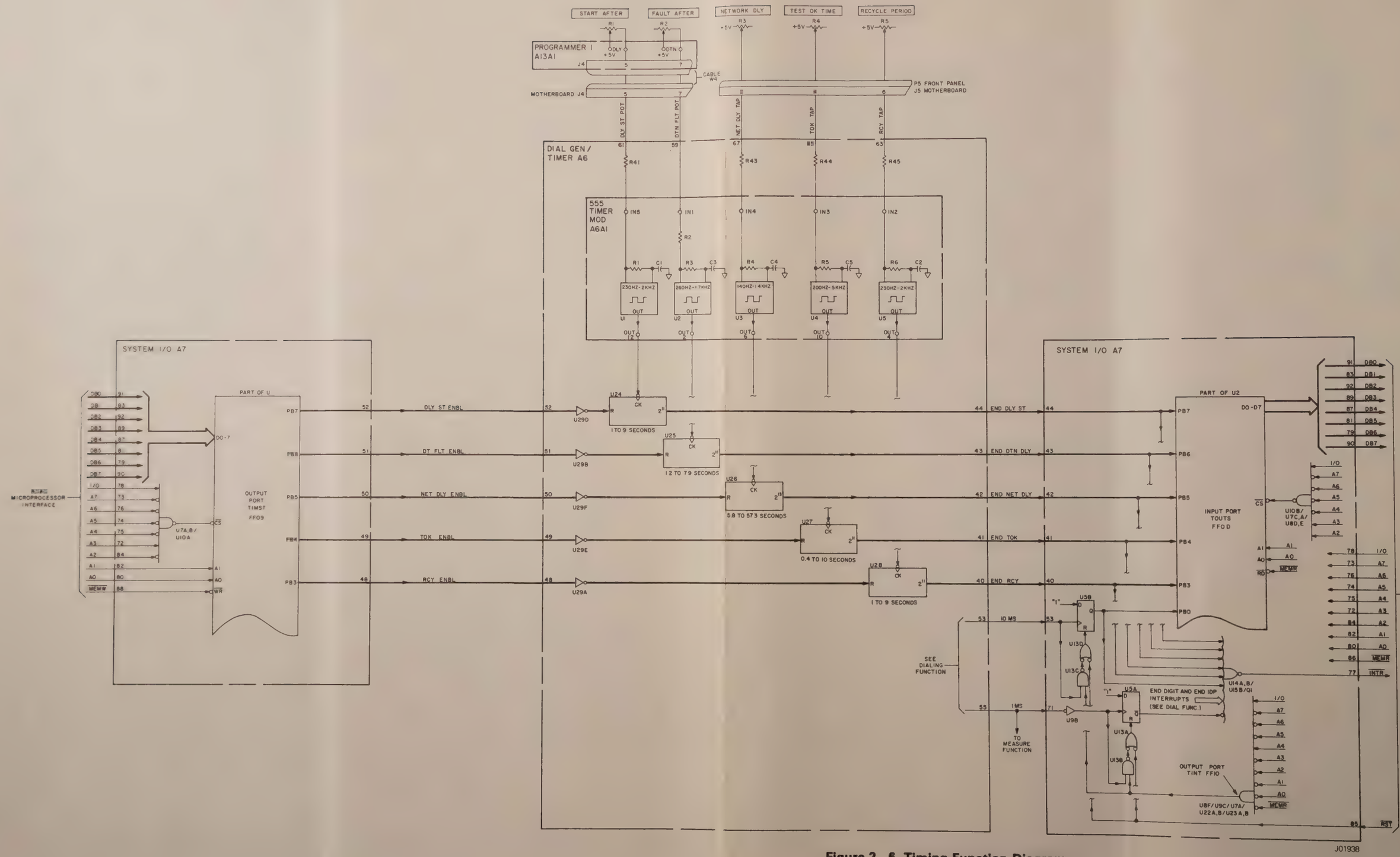
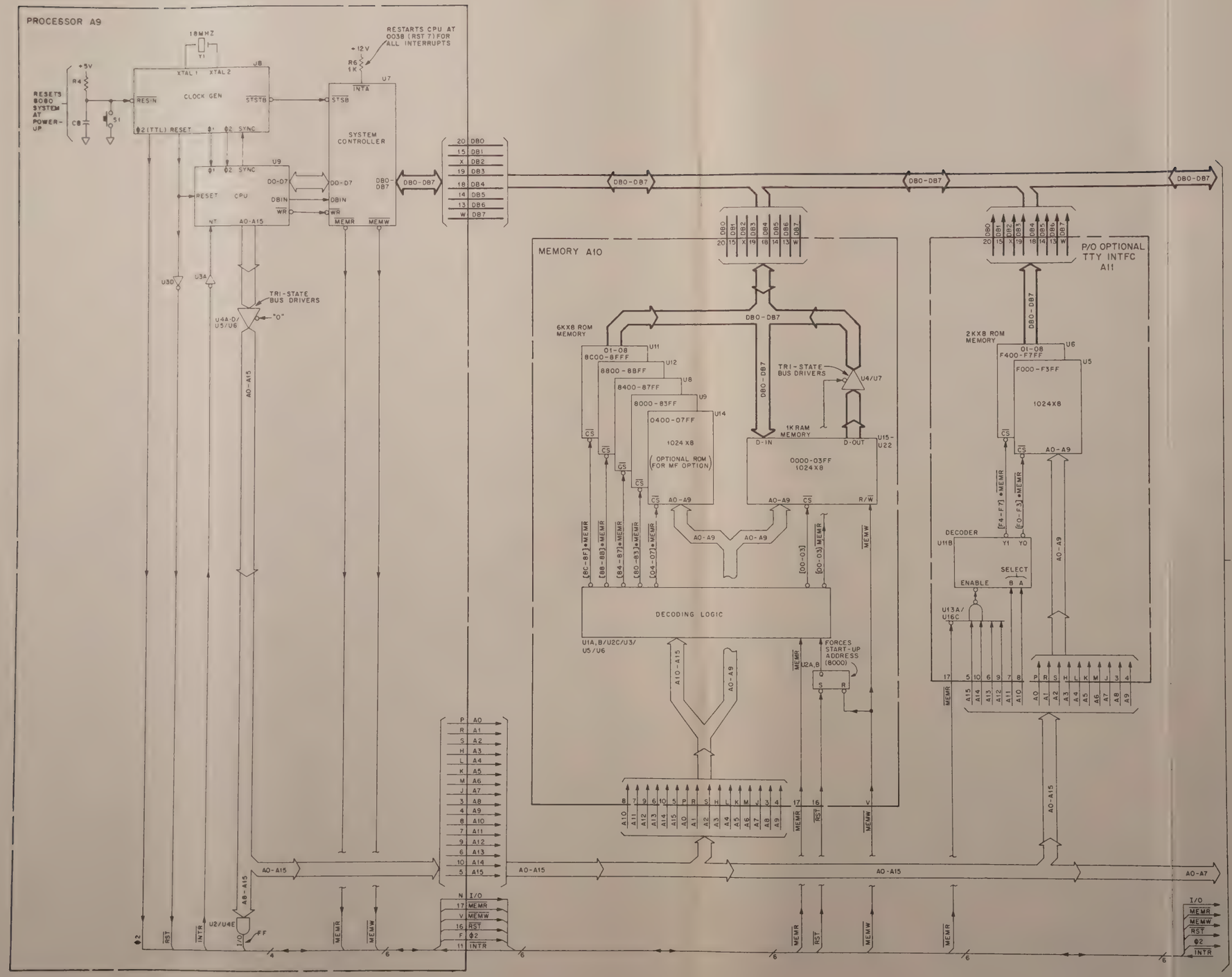


Figure 2—6. Timing Function Diagram.



INPUT PORTS

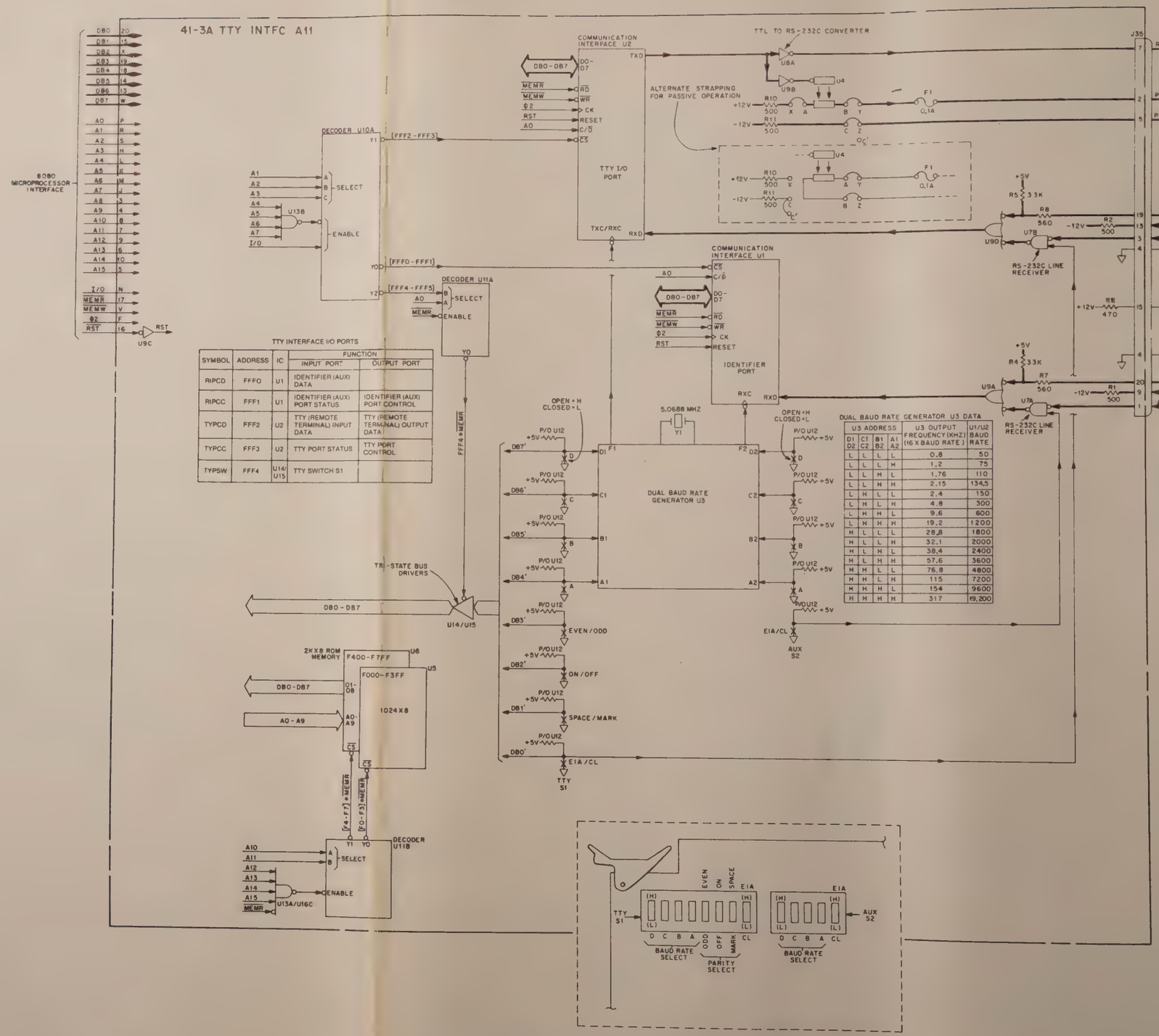
SYMBOL	ADDRESS	FUNCTION	FIGURE	
SWTCH	FFO2	SWITCH BUS		
DPORT	FFOA	TRACE/TEST SWITCHES	7-2	
TOUTS	FFOD	TIMEOUTS/END DIGIT, END IDP INTERRUPTS	7-3, 7-6	
DTCTP	FFOE	IDLE, BUSY STATUS/TONE PRESENCE DATA		
RIPCD	FFFO	IDENTIFIER (AUX) DATA PORT	7-7	P/O TELEPRINTER OPTION
RIPCC	FFF1	IDENTIFIER (AUX) STATUS PORT	7-7	
TYPCD	FFF2	TTY INPUT DATA PORT		
TYPCC	FFF3	TTY STATUS PORT	7-7	
TYPSW	FFF4	TTY SWITCH PORT		

OUTPUT PORTS

SYMBOL	ADDRESS	FUNCTION	FIGURE	
SGMNT	FFOO	SEGMENT/BRIGHTNESS CONTROL	7-5	
DCNT	FFO1	DIGIT MUX/SWITCH MUX/ LINE SELECT	7-2, 7-5	
ALAMP	FFO4	STATE LAMPS	7-5	
BLAMP	FFO5	TEST RESULT LAMPS	7-5	
CLAMP	FFO6	TEST RESULT LAMPS	7-5	
TTPRT	FFO8	TT/IMF ADDRESS BUS	7-3	
TIMST	FFO9	TIMERS START CONTROL/ DIALING MODE	7-3, 7-8	
DPORT	FFOA	DP DIGIT PORT	7-3	
STATP	FFOC	41-3A STATES/CHANNEL SELECT	7-2, 7-3, 7-4	
TINT	FFIO	CLEAR INTERRUPT HARDWARE	7-3, 7-8	
RIPCC	FFF1	IDENTIFIER (AUX) PORT CONTROL	7-7	P/O TELEPRINTER OPTION
TYPCD	FFF2	TTY OUTPUT DATA PORT	7-7	
TYPCC	FFF3	TTY PORT CONTROL		

J01968

Figure 2—7. Processing Function Diagram.



TTY INTERFACE I/O PORTS

SYMBOL	ADDRESS	IC	FUNCTION	
			INPUT PORT	OUTPUT PORT
RIPCD	FFF0	U1	IDENTIFIER (AUX) DATA	
RIPCC	FFF1	U1	IDENTIFIER (AUX) PORT STATUS	IDENTIFIER (AUX) PORT CONTROL
TYPCD	FFF2	U2	TTY (REMOTE TERMINAL) INPUT DATA	TTY (REMOTE TERMINAL) OUTPUT DATA
TYPCC	FFF3	U2	TTY PORT STATUS	TTY PORT CONTROL
TYPSW	FFF4	U14/ U15	TTY SWITCH S1	

DUAL BAUD RATE GENERATOR U3 DATA

U3 ADDRESS D1 D2	C1 C2	B1 B2	A1 A2	U3 OUTPUT FREQUENCY (KHZ) (16 X BAUD RATE)	U1/U2 BAUD RATE
L	L	L	L	0.8	50
L	L	L	H	1.2	75
L	L	H	L	1.76	110
L	L	H	H	2.15	134.5
L	H	L	L	2.4	150
L	H	L	H	4.8	300
L	H	H	L	9.6	600
L	H	H	H	19.2	1200
H	L	L	L	28.8	1800
H	L	L	H	32.1	2000
H	L	H	L	38.4	2400
H	L	H	H	57.6	3600
H	H	L	L	76.8	4800
H	H	L	H	115	7200
H	H	H	L	154	9600
H	H	H	H	317	19,200

Figure 2—8. Teleprinter Function Diagram.

TTS 41-3A STATE ROUTINES

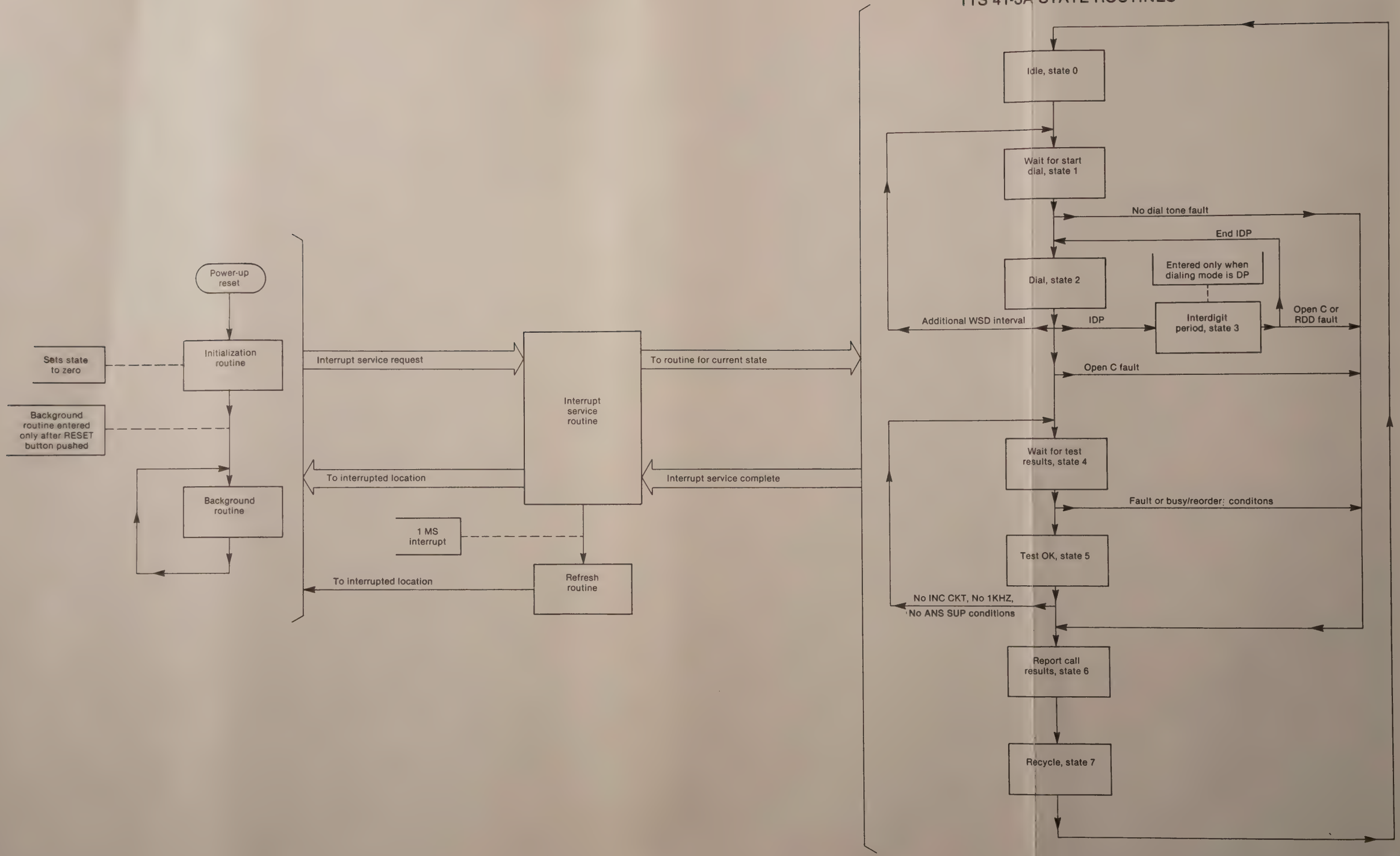


Figure 2—9. Software Structure Diagram.

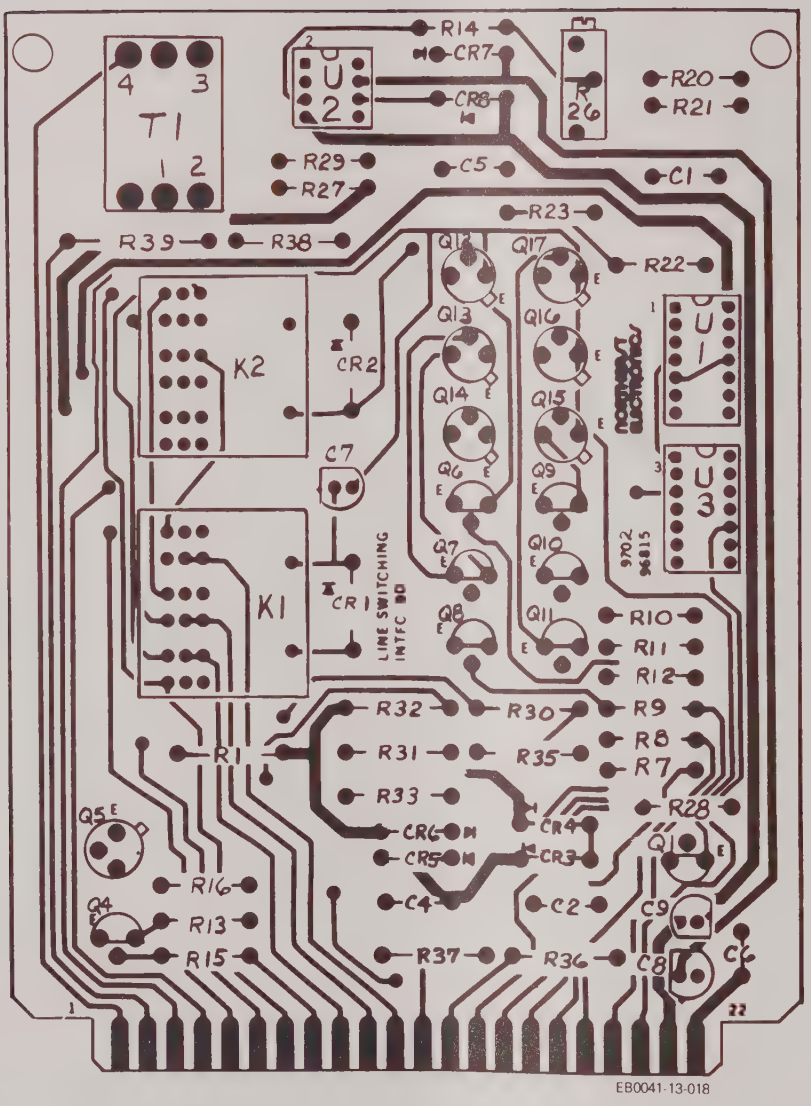
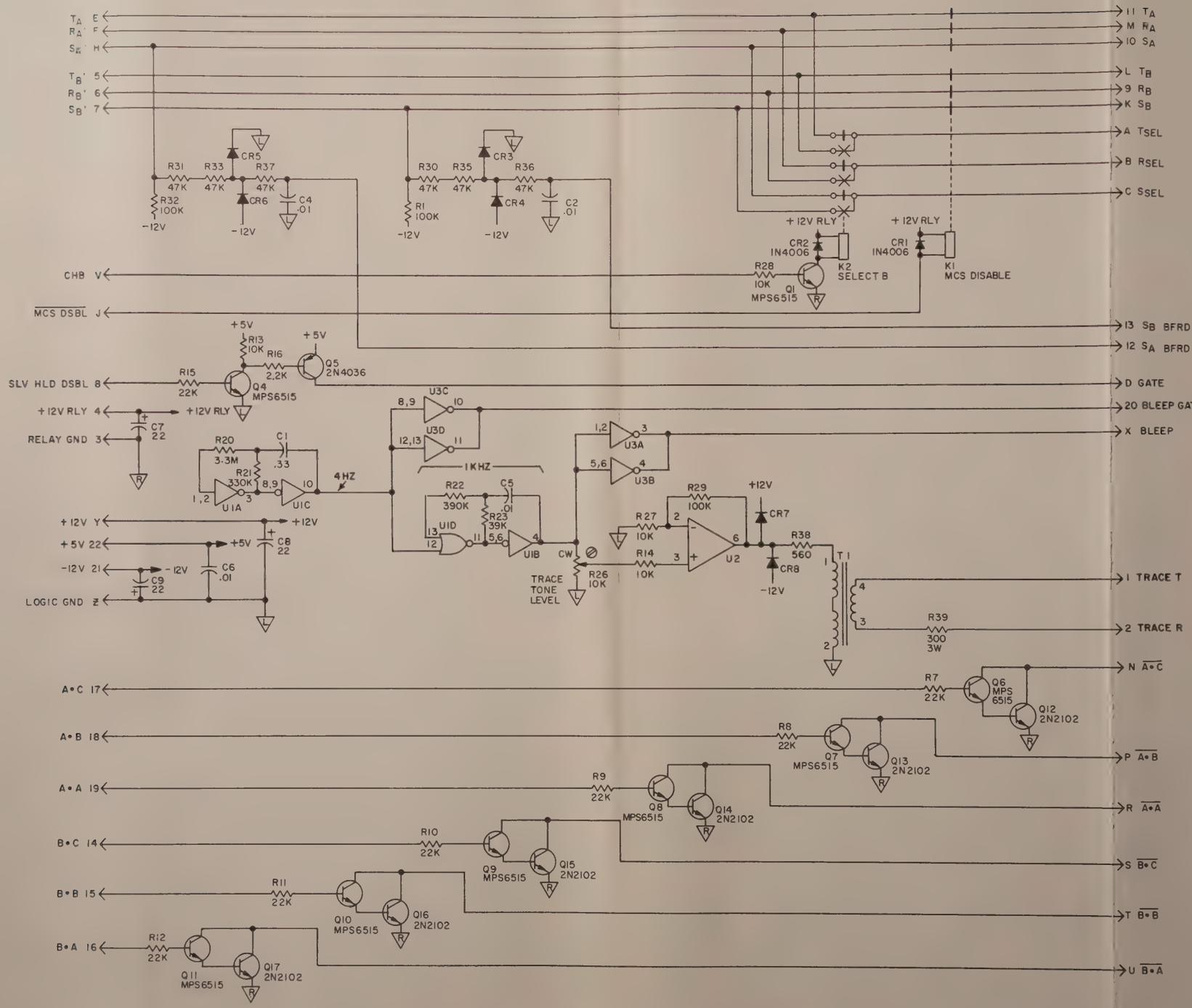


Figure 2—10. Line Switching Interface Component Location Diagram



IC DATA					
REF DES	TYPE	+5V	−12V	+12V	GND
U1,U3	CD4001	14	—	—	7
U2	LM741	—	4	7	—

LAST-USED REFERENCE DESIGNATIONS							
C9	R39	CR8	T1	K2	U3	Q17	

NOTES
1. CAPACITANCE IN MICROFARADS
2. ALL DIODES IN4148 UNLESS OTHERWISE SPECIFIED

ED0041 13-318

Line Switch Intfc.	
NE PART NO.	B0041-13-018
REF DESIG	A1
PC NO.	96815
CARD SLOT	1

Figure 2—11. Line Switching Interface Schematic Diagram.

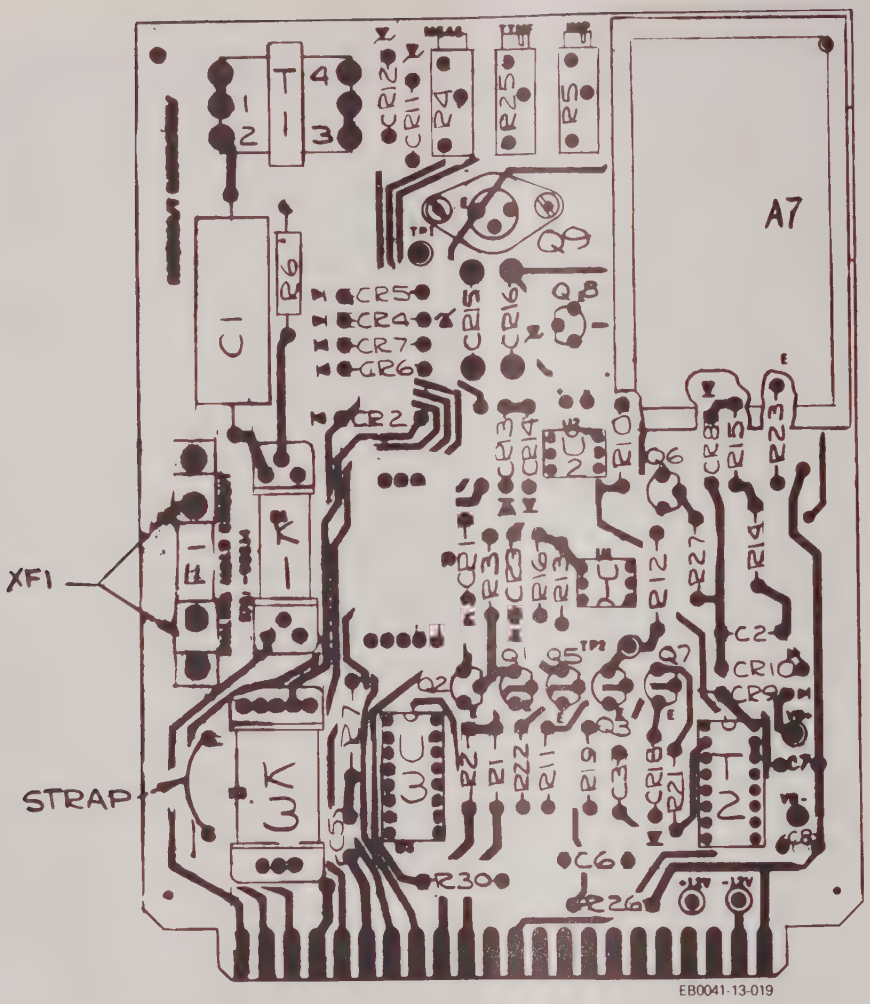


Figure 2—12. Dialing/Hold Component Location Diagram.

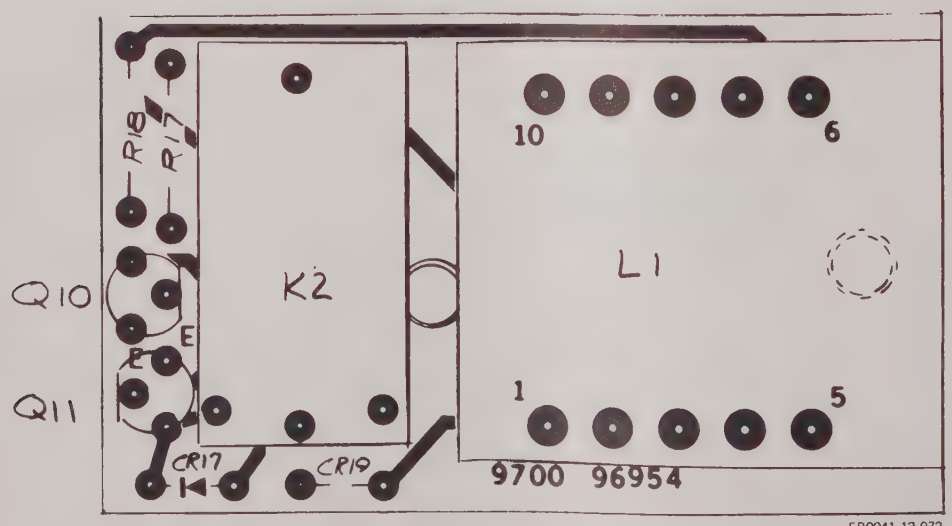
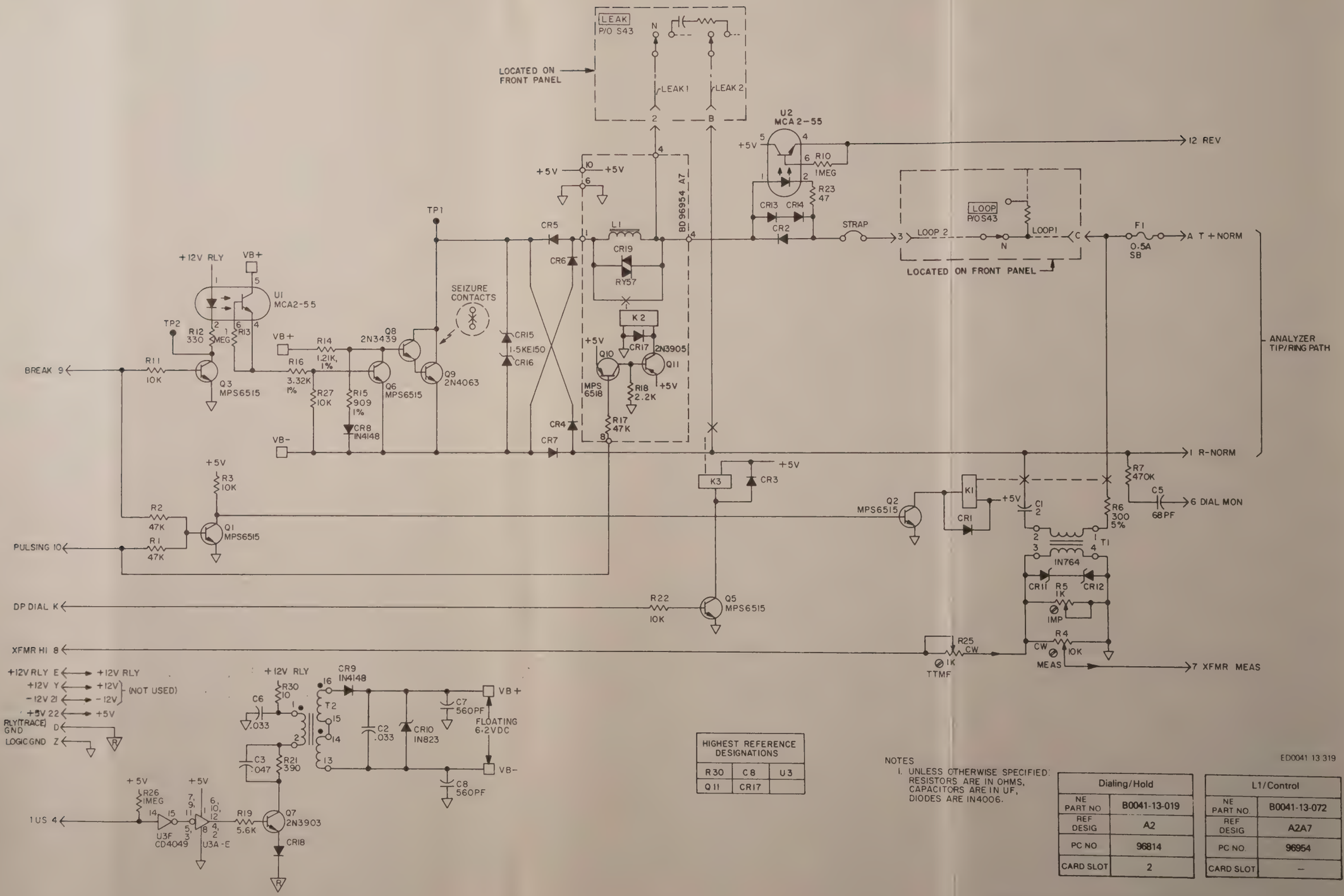


Figure 2—13. L1/Control Board Component Location Diagram.



HIGHEST REFERENCE DESIGNATIONS		
R30	C8	U3
Q11	CR17	

NOTES
1. UNLESS OTHERWISE SPECIFIED: RESISTORS ARE IN OHMS, CAPACITORS ARE IN UF, DIODES ARE IN4006.

ED0041 13 319

Dialing/Hold	
NE PART NO.	B0041-13-019
REF DESIG	A2
PC NO	96814
CARD SLOT	2

L1/Control	
NE PART NO.	B0041-13-072
REF DESIG	A2A7
PC NO.	96954
CARD SLOT	–

Figure 2–14. Dialing/Hold Schematic Diagram.

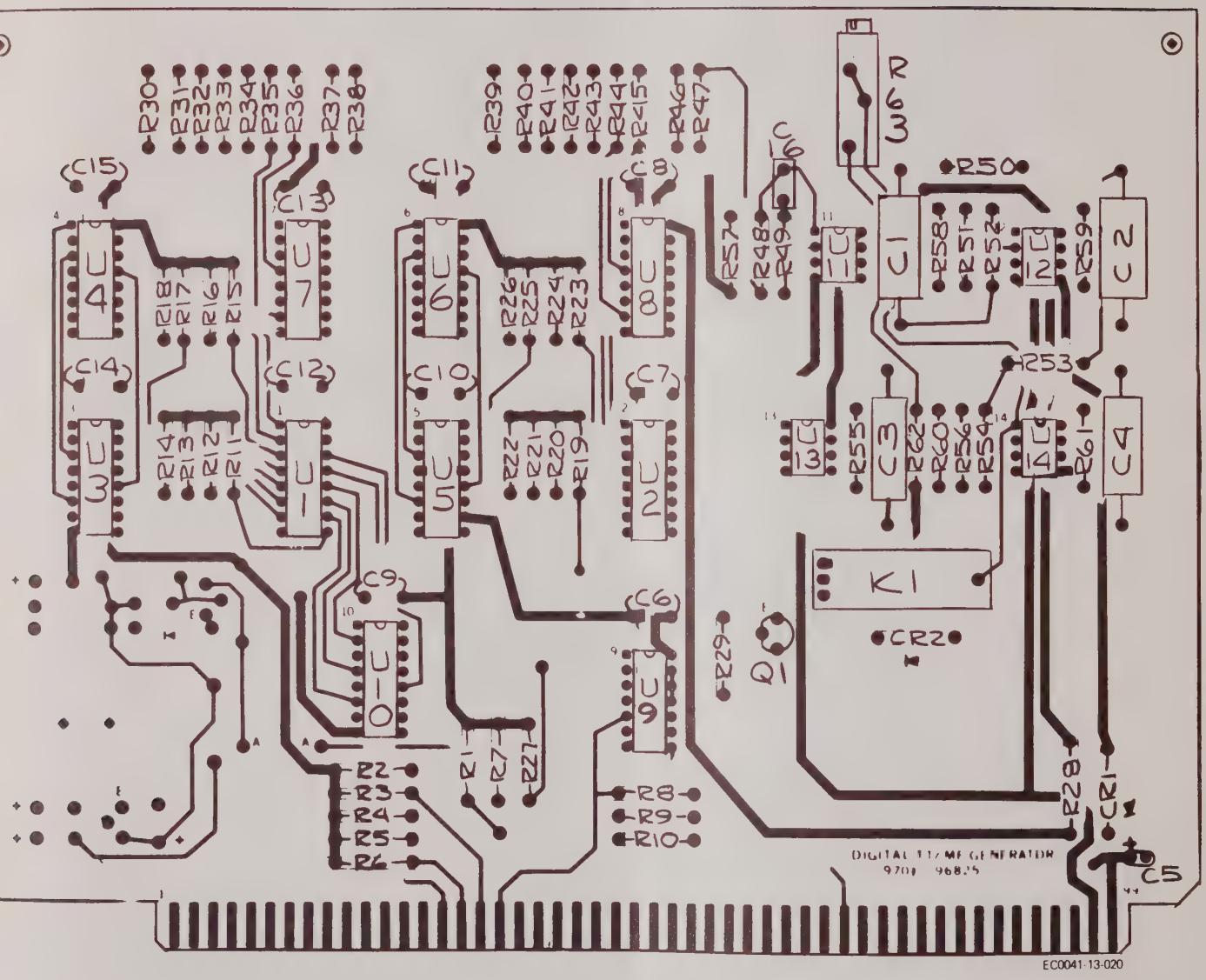
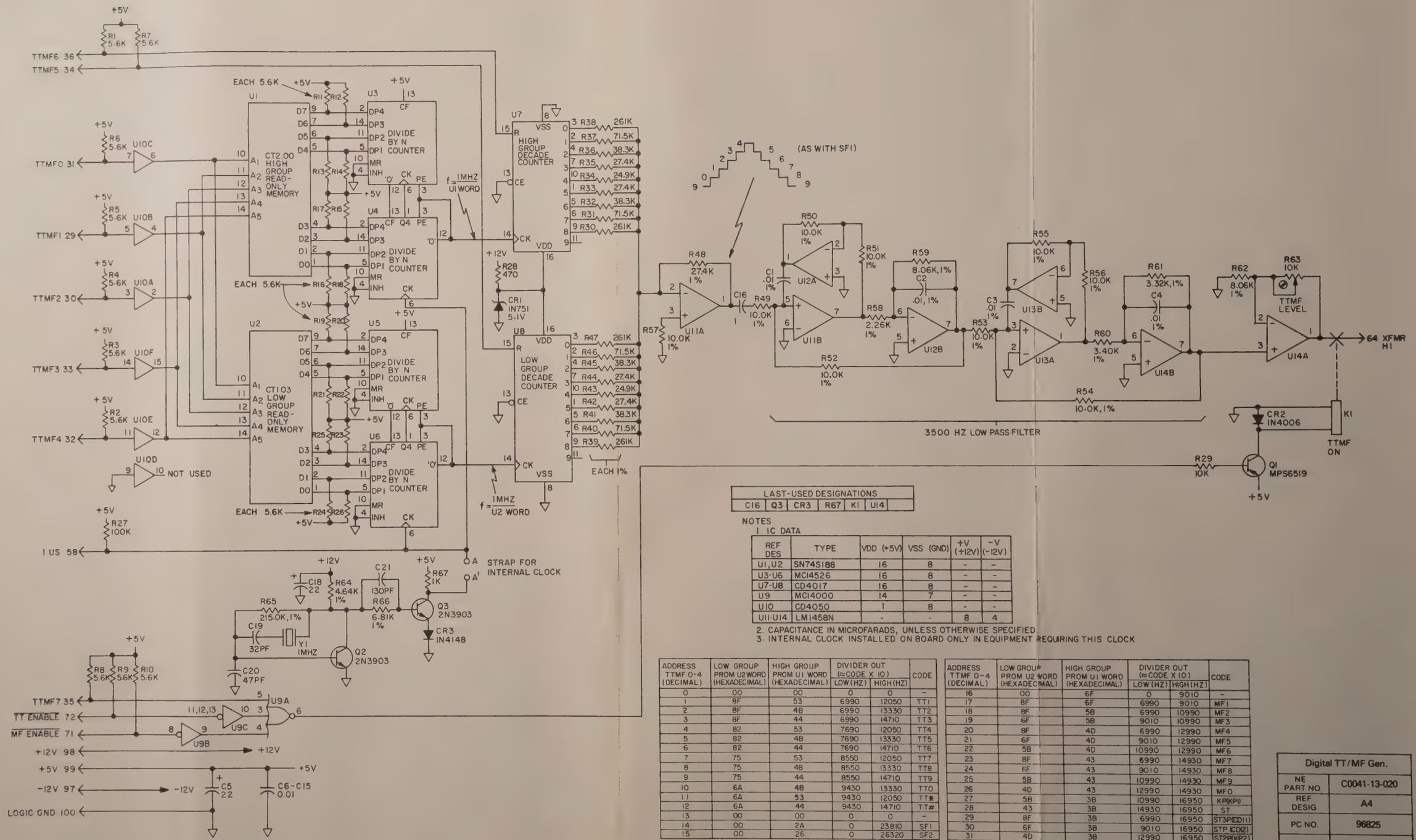


Figure 2—15. Digital TT/MF Generator Component Location Diagram.



LAST-USED DESIGNATIONS					
C16	Q3	CR3	R67	K1	U14

NOTES

1. IC DATA

REF DES	TYPE	VDD (+5V)	VSS (GND)	+V (+12V)	-V (-12V)
U1, U2	SN74S188	16	8	-	-
U3-U6	MC14526	16	8	-	-
U7-U8	CD4017	16	8	-	-
U9	MC14000	14	7	-	-
U10	CD4050	1	8	-	-
U11-U14	LM1458N	-	-	8	4

2. CAPACITANCE IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
3. INTERNAL CLOCK INSTALLED ON BOARD ONLY IN EQUIPMENT REQUIRING THIS CLOCK

ADDRESS TTMF 0-4 (DECIMAL)	LOW GROUP PROM U2 WORD (HEXADECIMAL)	HIGH GROUP PROM U1 WORD (HEXADECIMAL)	DIVIDER OUT (≈CODE X 10) LOW (HZ)	DIVIDER OUT (≈CODE X 10) HIGH (HZ)	CODE
0	00	00	0	0	-
1	8F	53	6990	12050	TT1
2	8F	48	6990	13330	TT2
3	8F	44	6990	14710	TT3
4	82	53	7690	12050	TT4
5	82	48	7690	13330	TT5
6	82	44	7690	14710	TT6
7	75	53	8550	12050	TT7
8	75	48	8550	13330	TT8
9	75	44	8550	14710	TT9
10	6A	48	9430	13330	TT0
11	6A	53	9430	12050	TT*
12	6A	44	9430	14710	TT#
13	00	00	0	0	-
14	00	2A	0	23810	SF1
15	00	26	0	26320	SF2

ADDRESS TTMF 0-4 (DECIMAL)	LOW GROUP PROM U2 WORD (HEXADECIMAL)	HIGH GROUP PROM U1 WORD (HEXADECIMAL)	DIVIDER OUT (≈CODE X 10) LOW (HZ)	DIVIDER OUT (≈CODE X 10) HIGH (HZ)	CODE
16	00	6F	0	9010	-
17	8F	6F	6990	9010	MF1
18	8F	5B	6990	10990	MF2
19	6F	5B	9010	10990	MF3
20	8F	4D	6990	12990	MF4
21	6F	4D	9010	12990	MF5
22	5B	4D	10990	12990	MF6
23	8F	43	6990	14930	MF7
24	6F	43	9010	14930	MF8
25	5B	43	10990	14930	MF9
26	4D	43	12990	14930	MF0
27	5B	3B	10990	16950	KP(KP1)
28	43	3B	14930	16950	ST
29	8F	3B	6990	16950	ST3P(CD11)
30	6F	3B	9010	16950	STP (CD12)
31	4D	3B	12990	16950	ST2P(KP2)

ED0041-13-320

Digital TT/MF Gen.	
NE PART NO.	C0041-13-020
REF DESIG	A4
PC NO.	96825
CARD SLOT	4

Figure 2—16. Digital TT/MF Generator Schematic Diagram.

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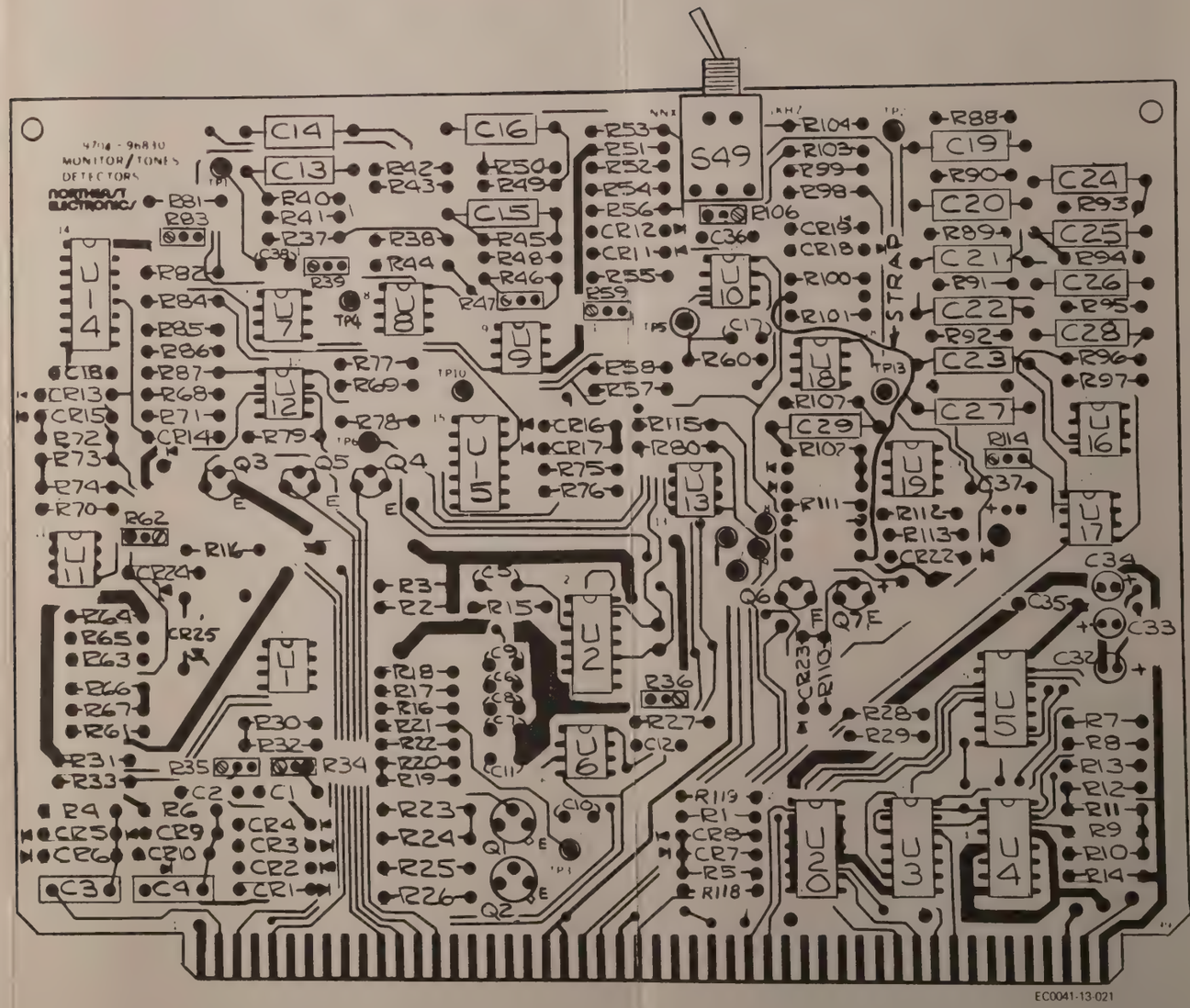
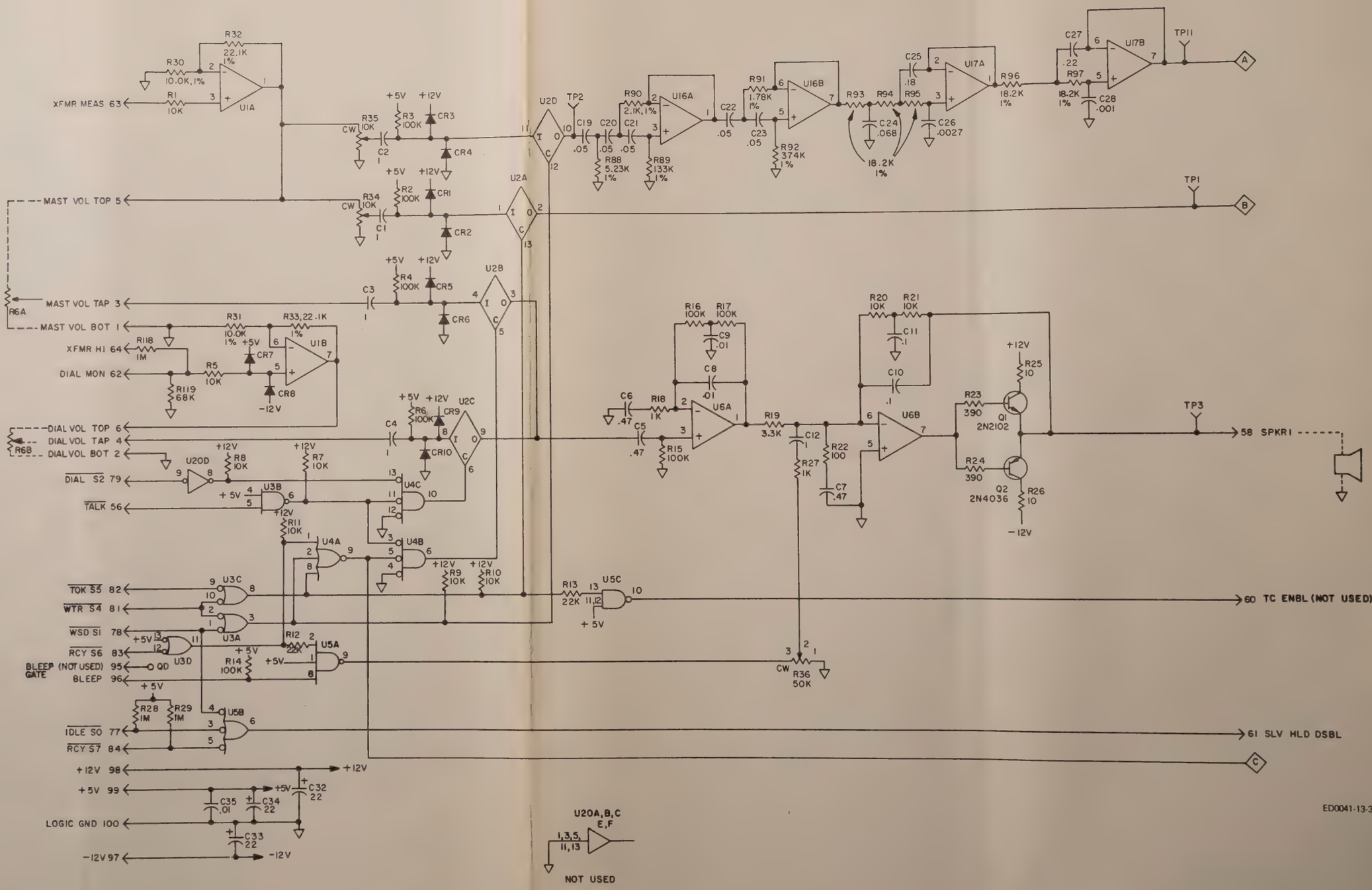
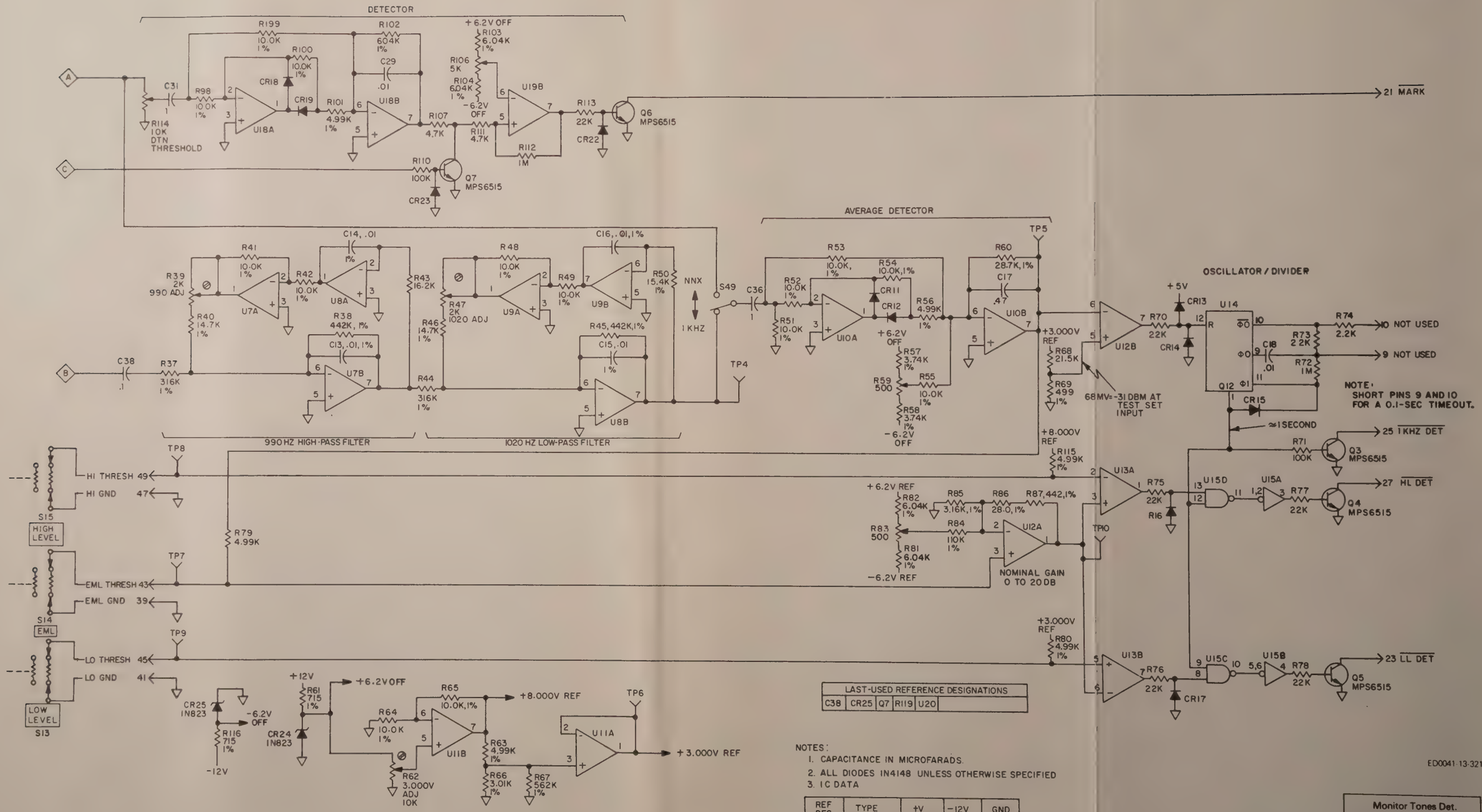


Figure 2—17. Monitor Tones Detector Component Location Diagram.



ED0041-13-321

Figure 2—18. Monitor Tones Detector Schematic Diagram (Sheet 1 of 2).



LAST-USED REFERENCE DESIGNATIONS				
C38	CR25	Q7	R119	U20

NOTES:
1. CAPACITANCE IN MICROFARADS.
2. ALL DIODES IN4148 UNLESS OTHERWISE SPECIFIED
3. IC DATA

REF DES	TYPE	+V	-12V	GND
U1	LM1458N	8(+12V)	4	-
U2	CD4066	14(+12V)	-	7
U3	74LS26	14(+5V)	-	7
U4	CD4025	14(+12V)	-	7
U5	CD4023	14(+5V)	-	7
U6-U13	LM1458N	8(+12V)	4	-
U14	CD4060	16(+5V)	-	8
U15	CD4011	14(+5V)	-	7
U16-U19	LM1458N	8(+12V)	4	-
U20	SN7407N	14(+5V)	-	7

ED0041-13-321

Monitor Tones Det.	
NE PART NO.	C0041-13-021
REF DESIG	A5
PC NO.	96830
CARD SLOT	5

Figure 2—18. Monitor Tones Detector Schematic Diagram (Sheet 2 of 2).

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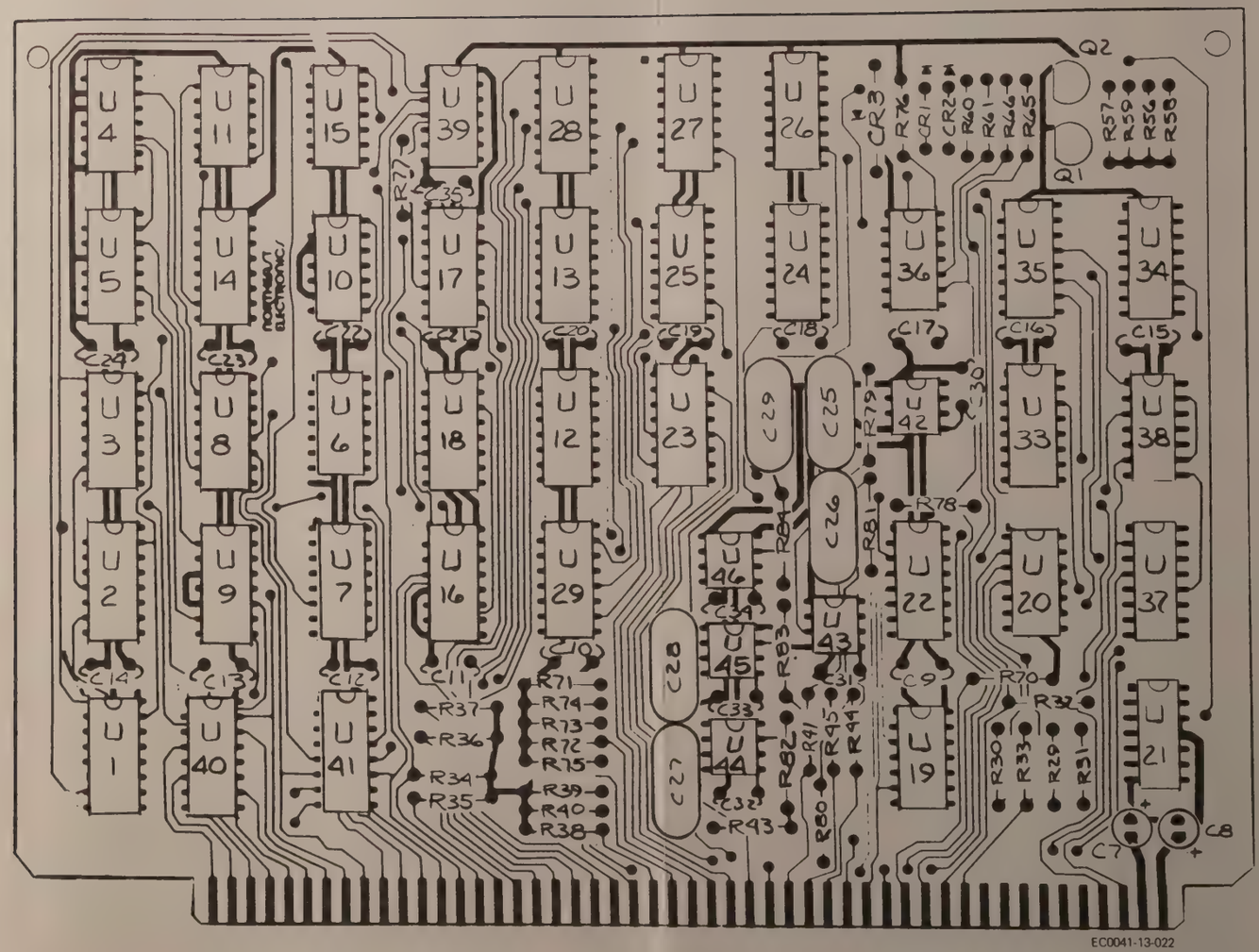


Figure 2—19. Dial Control/Timer Component Location Diagram.

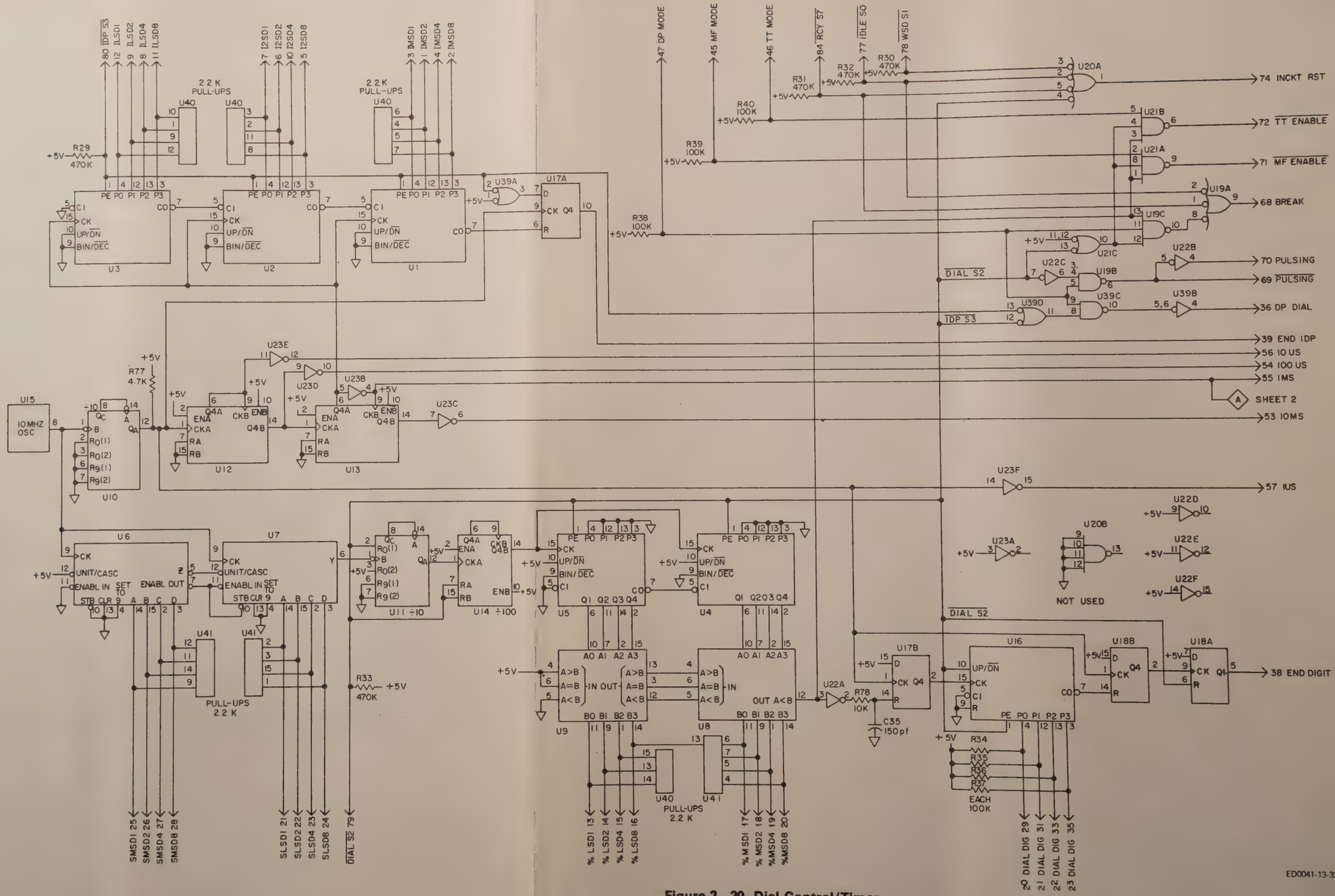
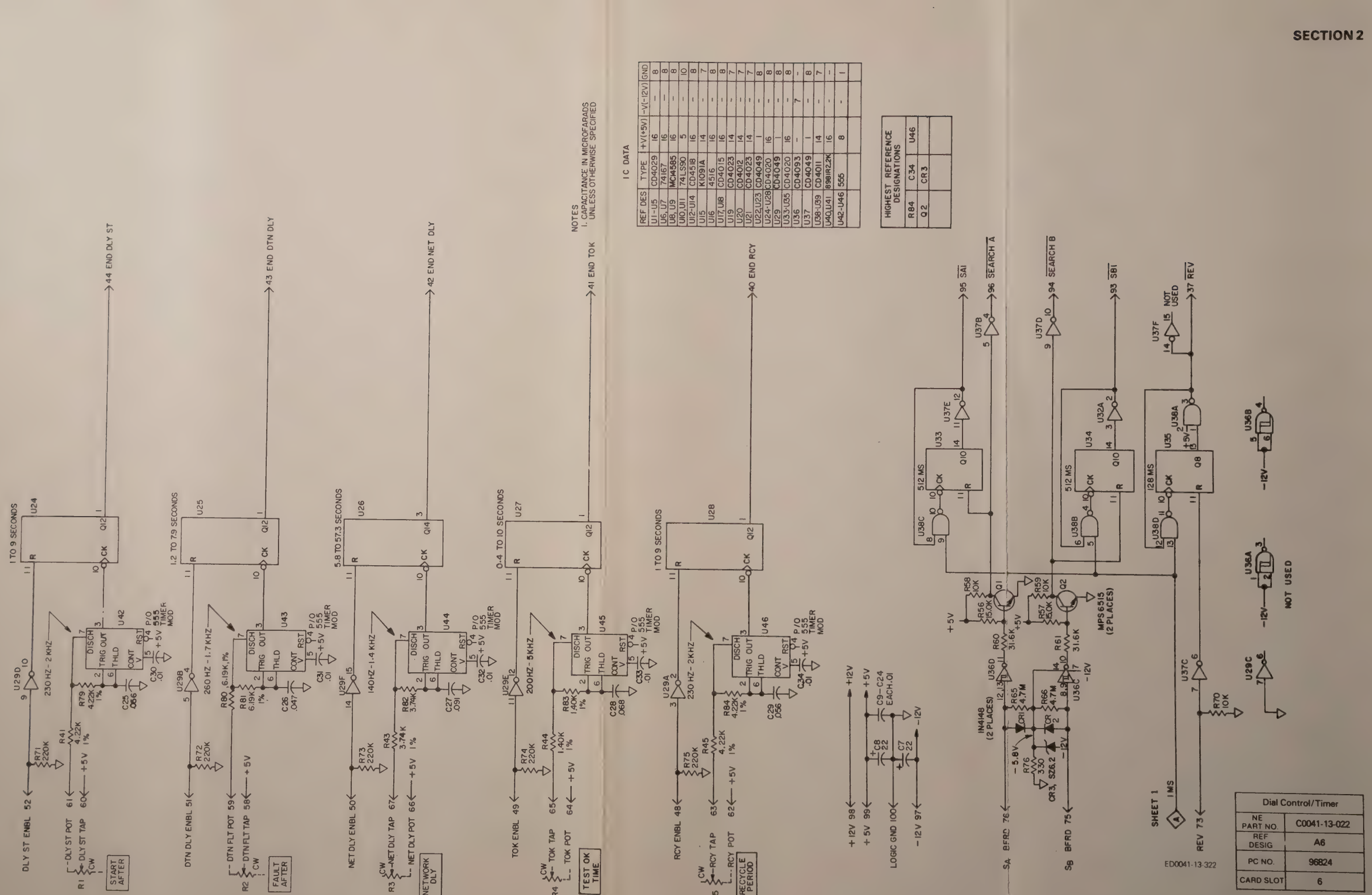


Figure 2—20. Dial Control/Timer Schematic Diagram (Sheet 1 of 2).



REF DES	TYPE	+V(+5V)	-V(-12V)	GND
U1-U5	CD4029	16	-	8
U6, U7	74167	16	-	8
U8, U9	MC4585	16	-	8
U10, U11	74LS90	5	-	10
U12-U14	CD4518	16	-	8
U15	K1091A	14	-	7
U16	4516	16	-	8
U17, U18	CD4015	16	-	8
U19	CD4023	14	-	7
U20	CD4012	14	-	7
U21	CD4023	14	-	7
U22, U23	CD4049	1	-	8
U24-U28	CD4020	16	-	8
U29	CD4049	1	-	8
U33-U35	CD4020	16	-	8
U36	CD4093	-	7	-
U37	CD4049	1	-	8
U39-U39	CD4011	14	-	7
U40, U41	8981R2.2K	16	-	-
U42-U46	555	8	-	1

Figure 2—20. Dial Control/Timer Schematic Diagram (Sheet 2 of 2).

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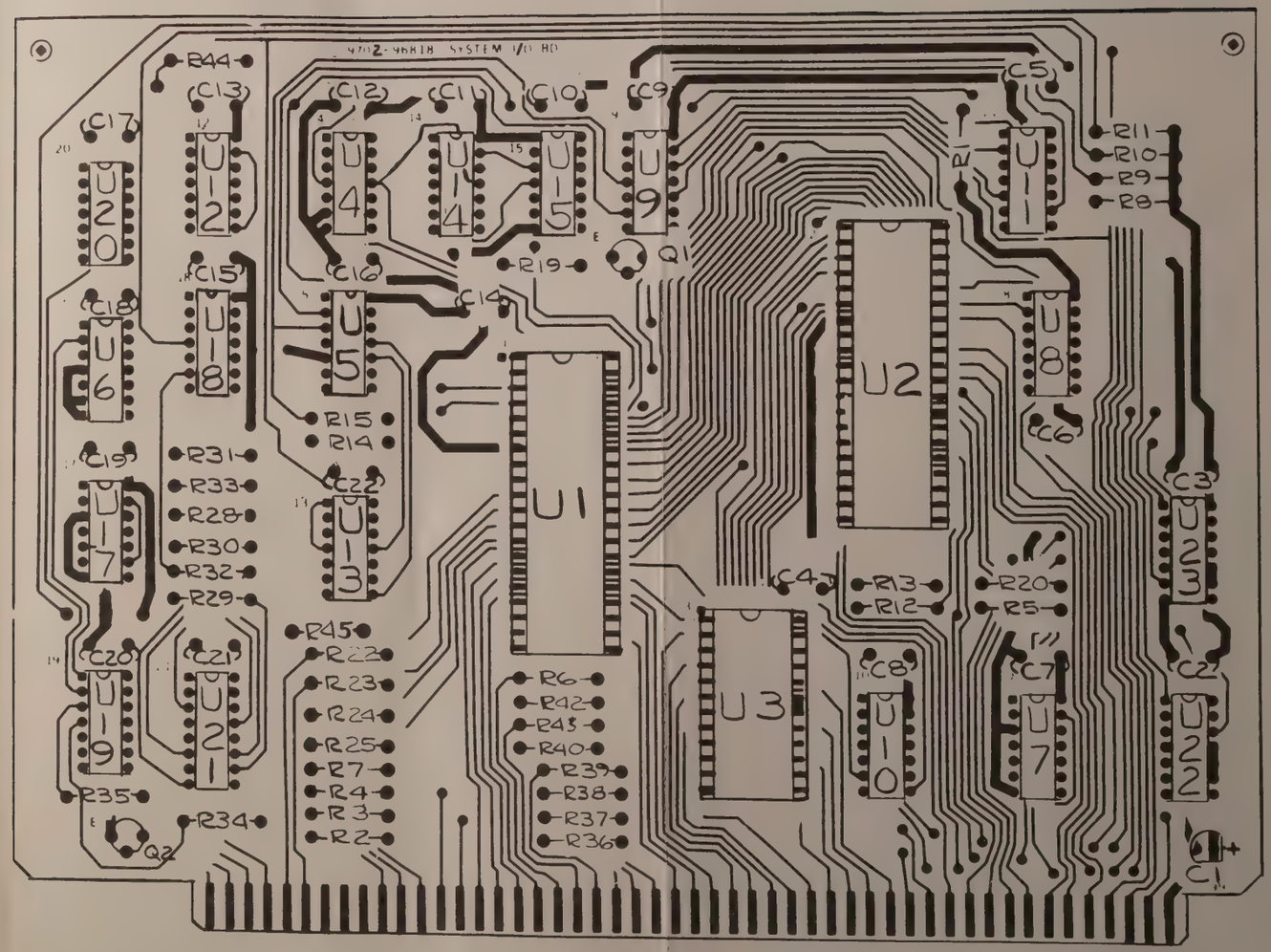
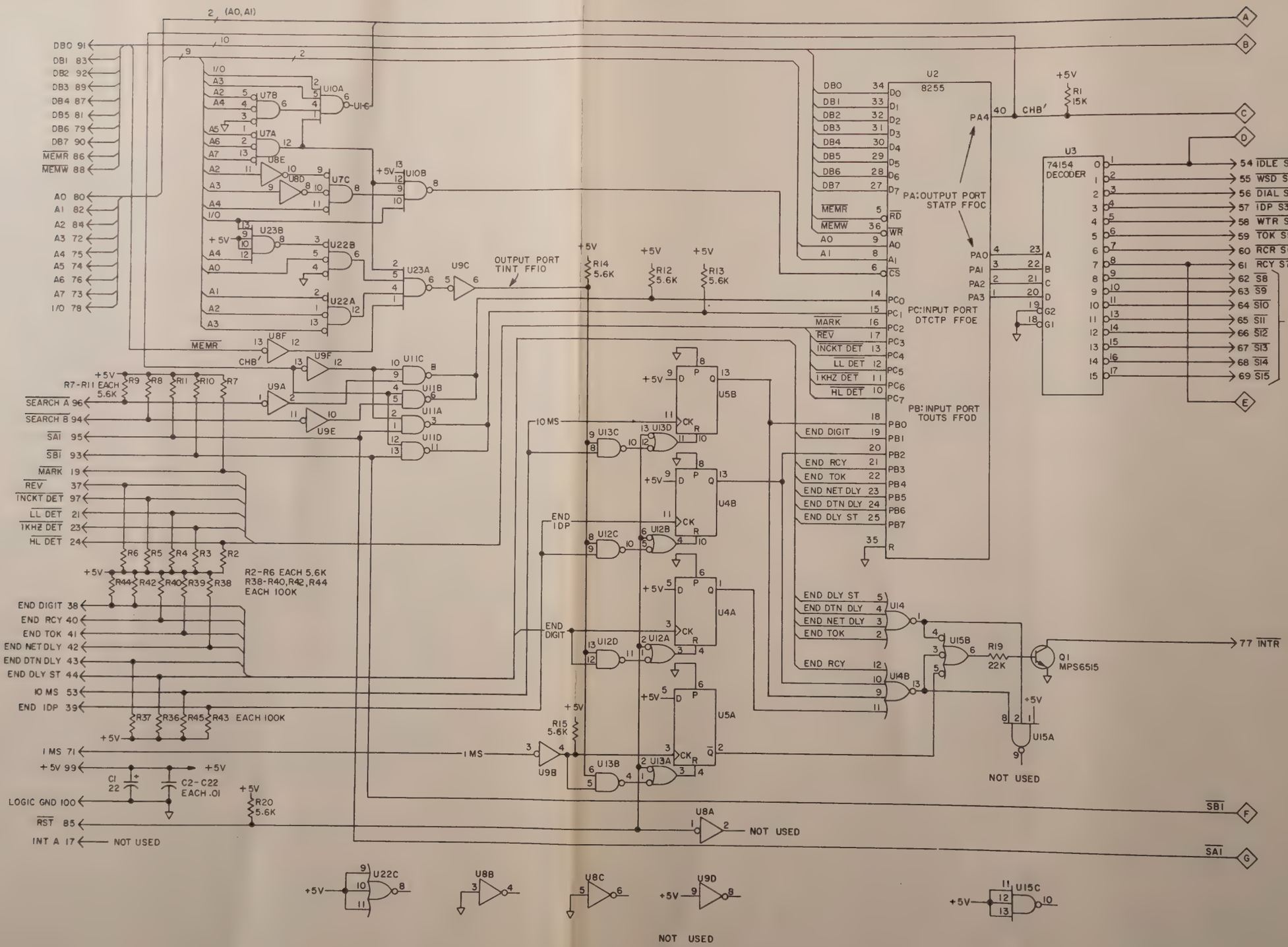


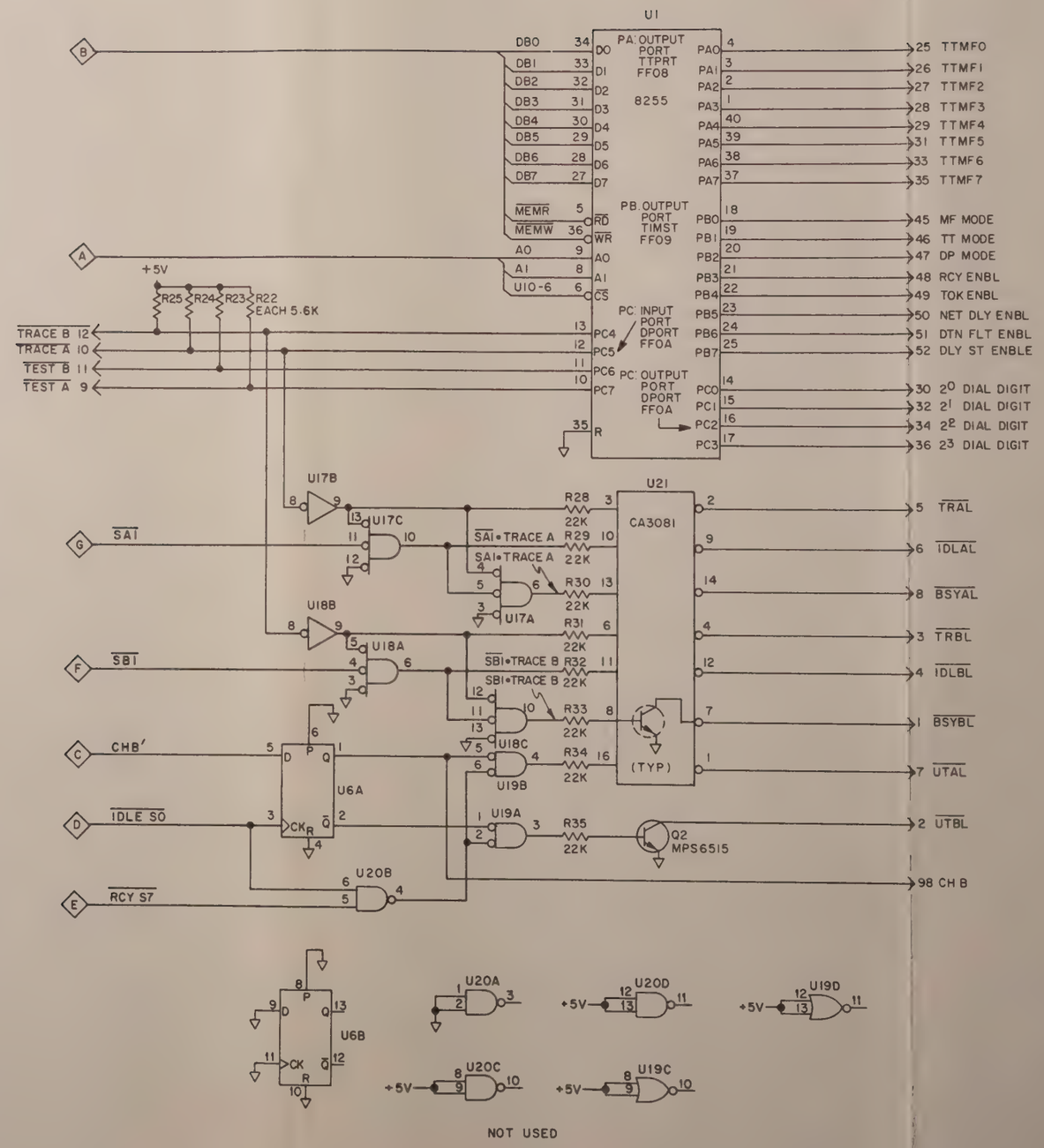
EC0041-13-023

Figure 2—21. System I/O Board Component Location Diagram.



ED0041-13-323

Figure 2–22. System I/O Board Schematic Diagram (Sheet 1 of 2)



LAST-USED REFERENCE DESIGNATIONS				
C22	Q2	R45	U23	

NOTES:
1. CAPACITANCE IN MICROFARADS
2 IC DATA

REF DES	TYPE	+V(+5V)	GND
U1,U2	8255	26	7
U3	74154	24	12
U4-U6	CD4013	14	7
U7	74LS27	14	7
U8,U9	74LS04	14	7
U10	74LS20	14	7
U11	74LS03	14	7
U12,U13	CD4011	14	7
U14	CD4002	14	7
U15	CD4023	14	7
U17,U18	CD4000	14	7
U19	CD4001	14	7
U20	CD4011	14	7
U21	CA3081		5,15
U22	74LS27	14	7
U23	74LS20	14	7

ED0041-130323

System I/O	
NE PART NO.	C0041-13-023
REF DESIG	A7
PC NO.	96818
CARD SLOT	7

Figure 2—22. System I/O Board Schematic Diagram (Sheet 2 of 2).

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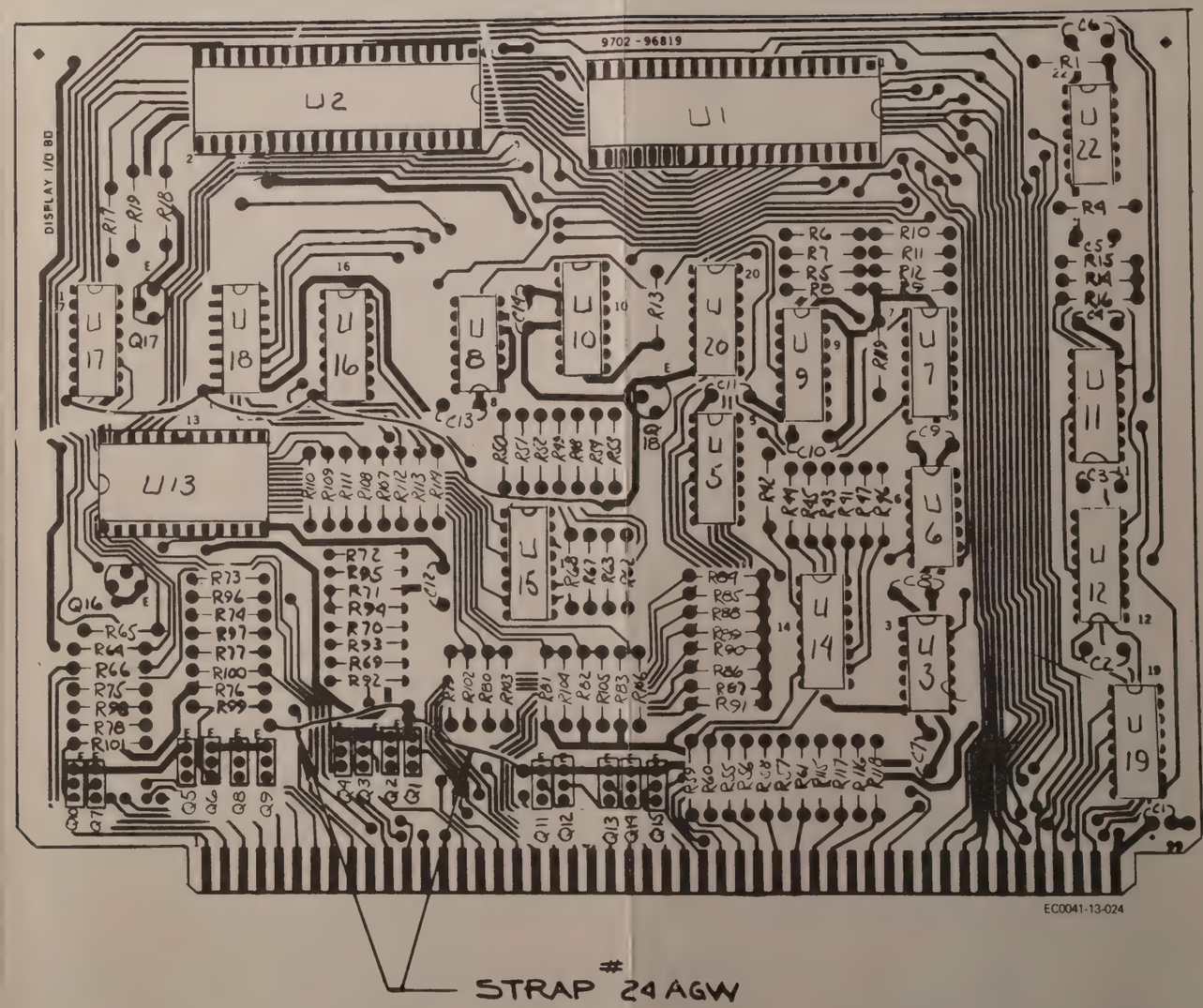


EC0041-13-024

Figure 2—23. Display I/O Board Component Location Diagram.

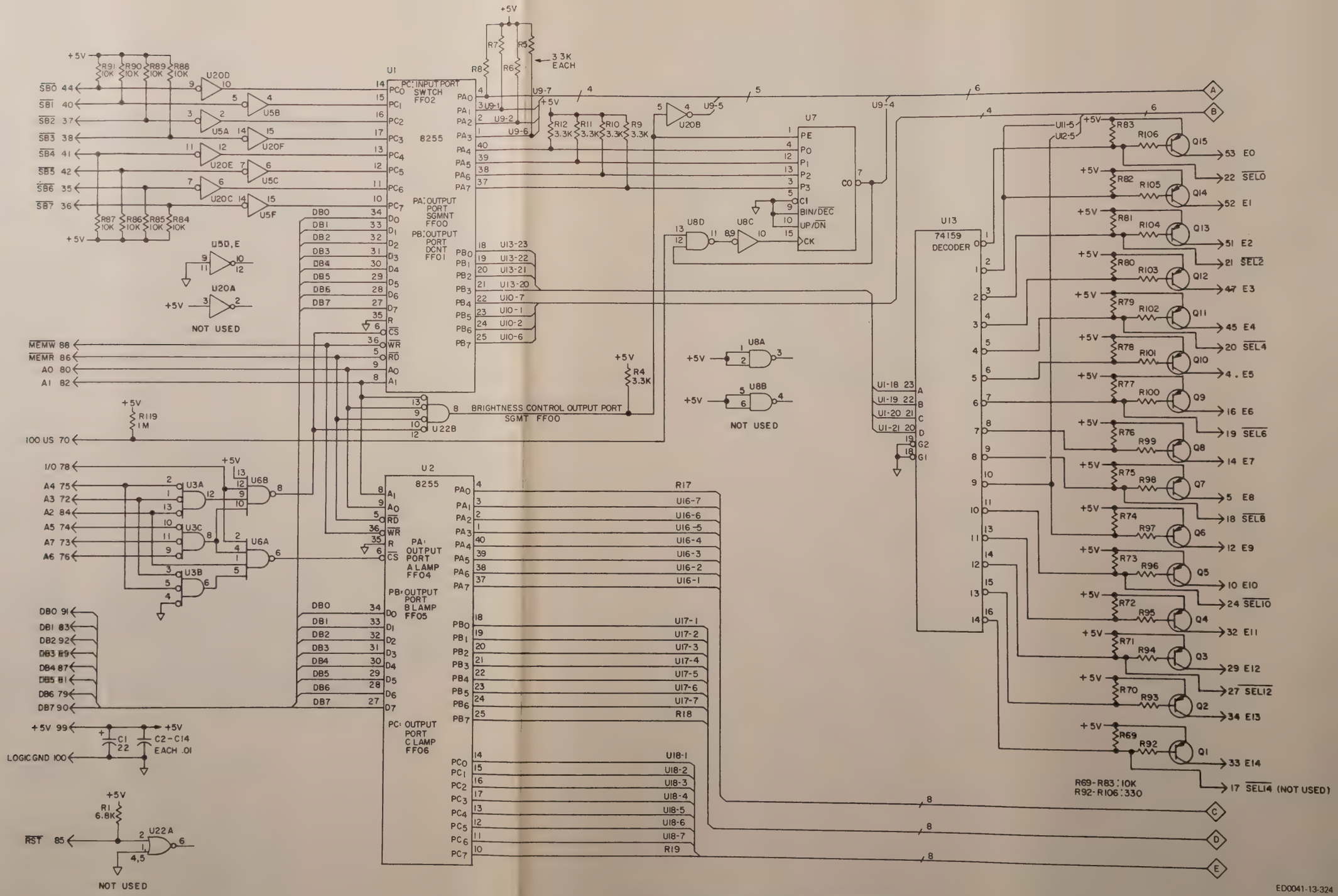
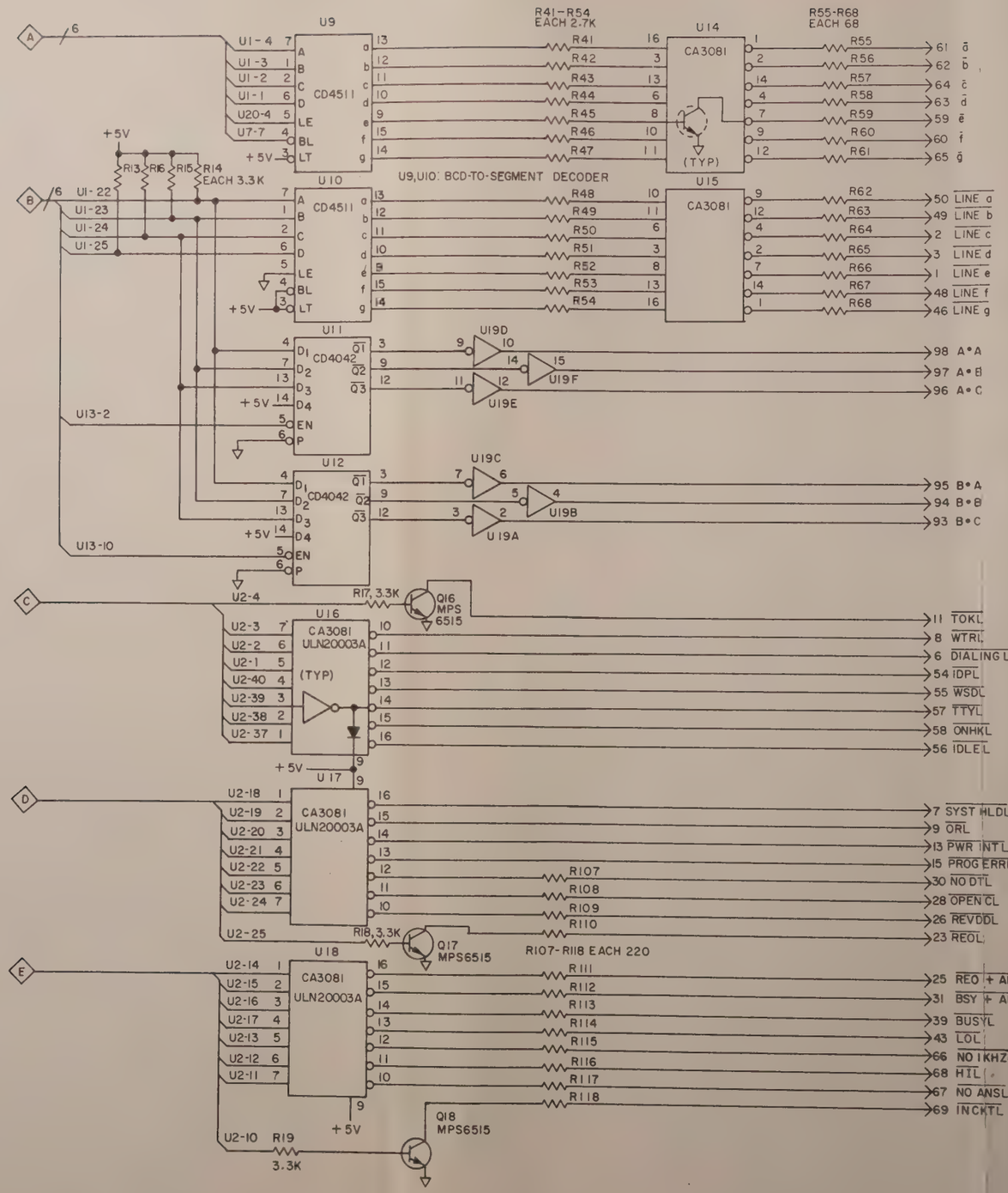


Figure 2—24. Display I/O Board Schematic Diagram (Sheet 1 of 2).



LAST-USED REFERENCE DESIGNATIONS				
C14	Q15	R119	U22	

NOTES
1. CAPACITANCE IN MICROFARADS
2. ALL TRANSISTORS MJE371 UNLESS OTHERWISE SPECIFIED
3. I C DATA

REF DES	TYPE	VDD (+5V)	GND
U1, U2	8255	26	7
U3	74LS27	14	7
U5	CD4049	1	8
U6	74LS20	14	7
U7	CD4029	16	8
U8	CD4011	14	7
U9, U10	CD4511	16	8
U11, U12	CD4042	16	8
U13	SN74159	24	12
U14, U15	CA3081	-	5, 15
U19, U20	CD4049	1	8
U22	SN7425	14, 11, 3	7
U16-U18	ULN20003A	-	8

Display I/O	
NE PART NO.	C0041-13-024
REF DESIG	A8
PC NO.	96819
CARD SLOT	8

ED0041-13-324

Figure 2—24. Display I/O Board Schematic Diagram (Sheet 2 of 2).

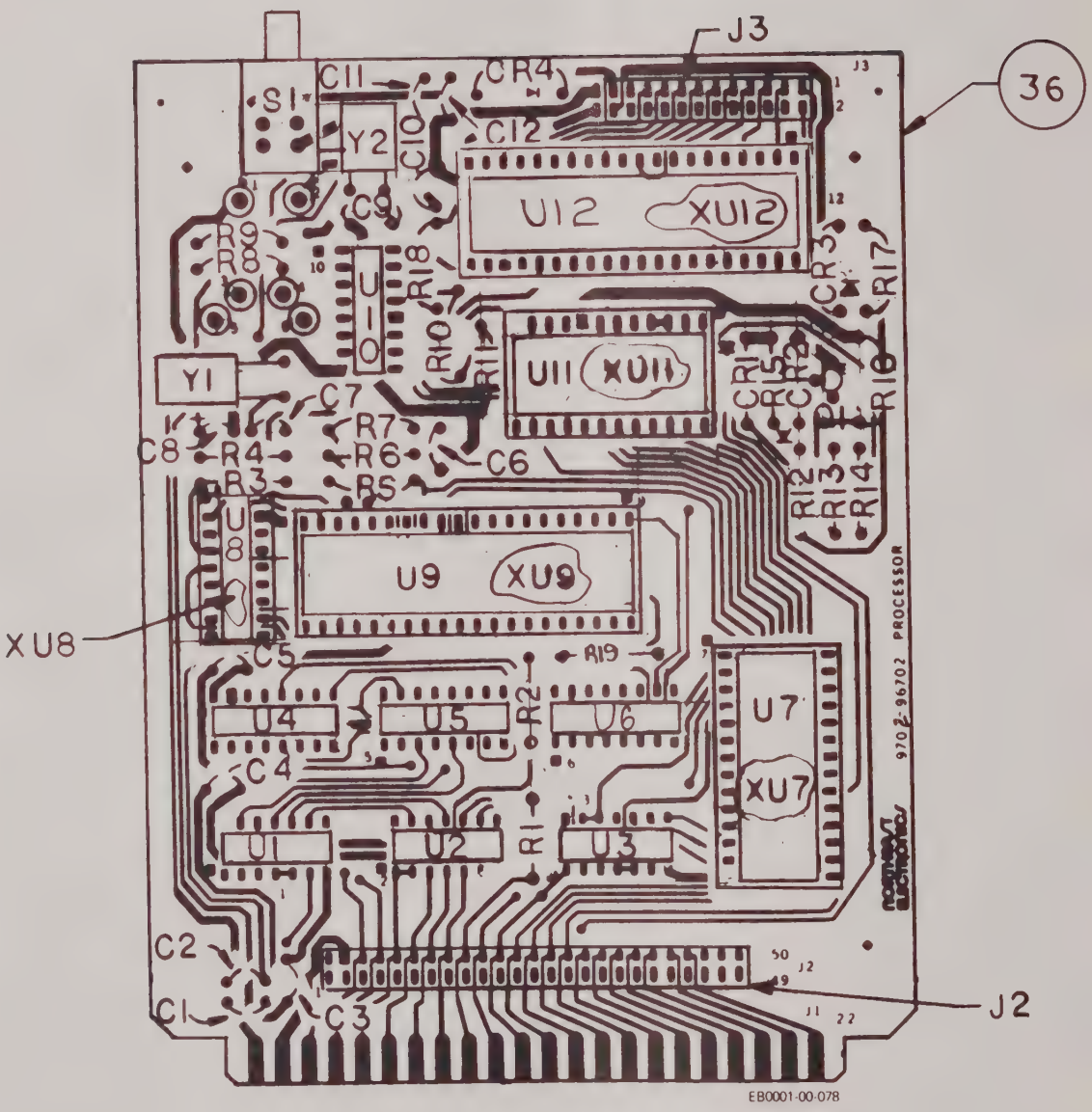


Figure 2—25. Processor Component Location Diagram.

NOTES
1. CONNECTORS J2 AND J3 ARE NORMALLY NOT USED.
2. SYMBOL ⊙ DENOTES QUICK-DISCONNECT POST.
3. CAPACITANCE IN MICROFARADS.
4. IC DATA

REF DES	TYPE	+12V	+5V	GND	-5V
U1, U2	74LS15	-	14	7	-
U3	7400	-	14	7	-
U4-U6	74367	-	16	8	-
U7	8228	-	28	14	-
U8	8224	9	16	8	-
U9	8080	28	20	2	11
U10	CD4060	16	-	8	-
U11	MC6850	-	12	1	-
U12	MC6820	-	20	1	-

LAST-USED REFERENCE DESIGNATION						
C12	CR4	Q1	R19	S1	U12	

Processor	
NE PART NO.	B0001-01-078
REF DESIG	A9
PC NO.	96702
CARD SLOT	9

ED0041 13:308

Figure 2—26. Processor Schematic Diagram.

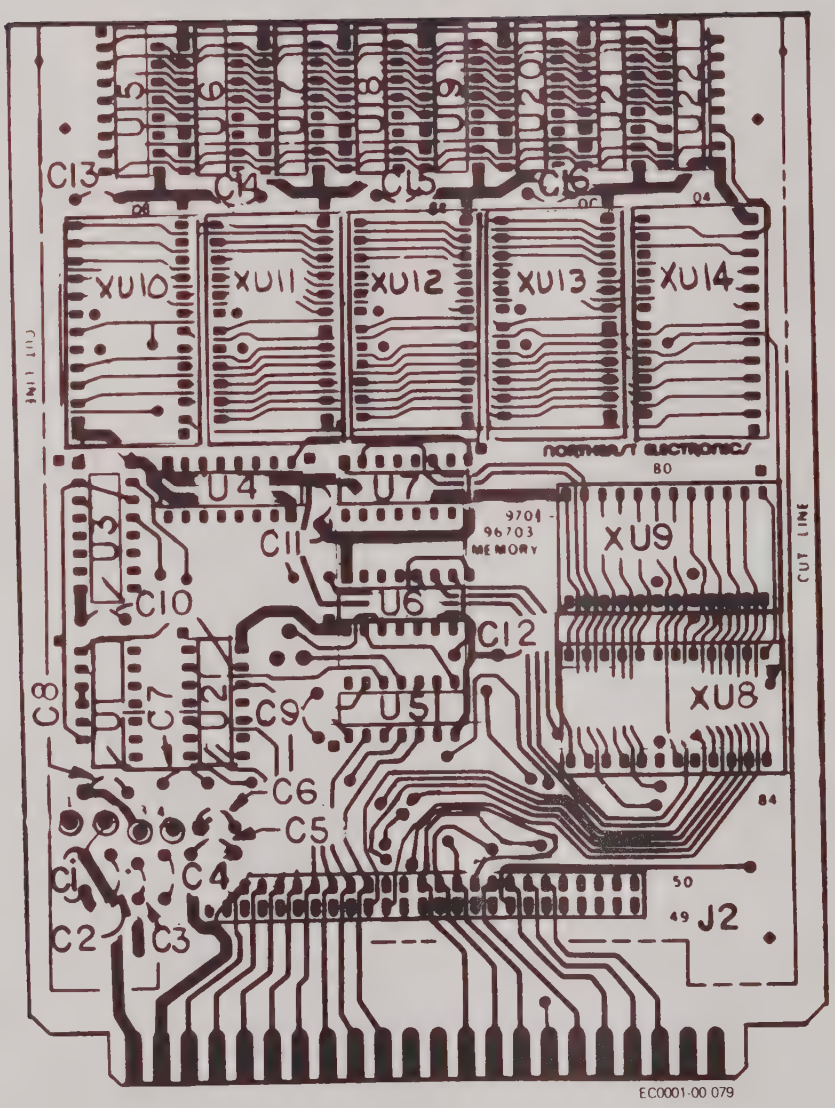
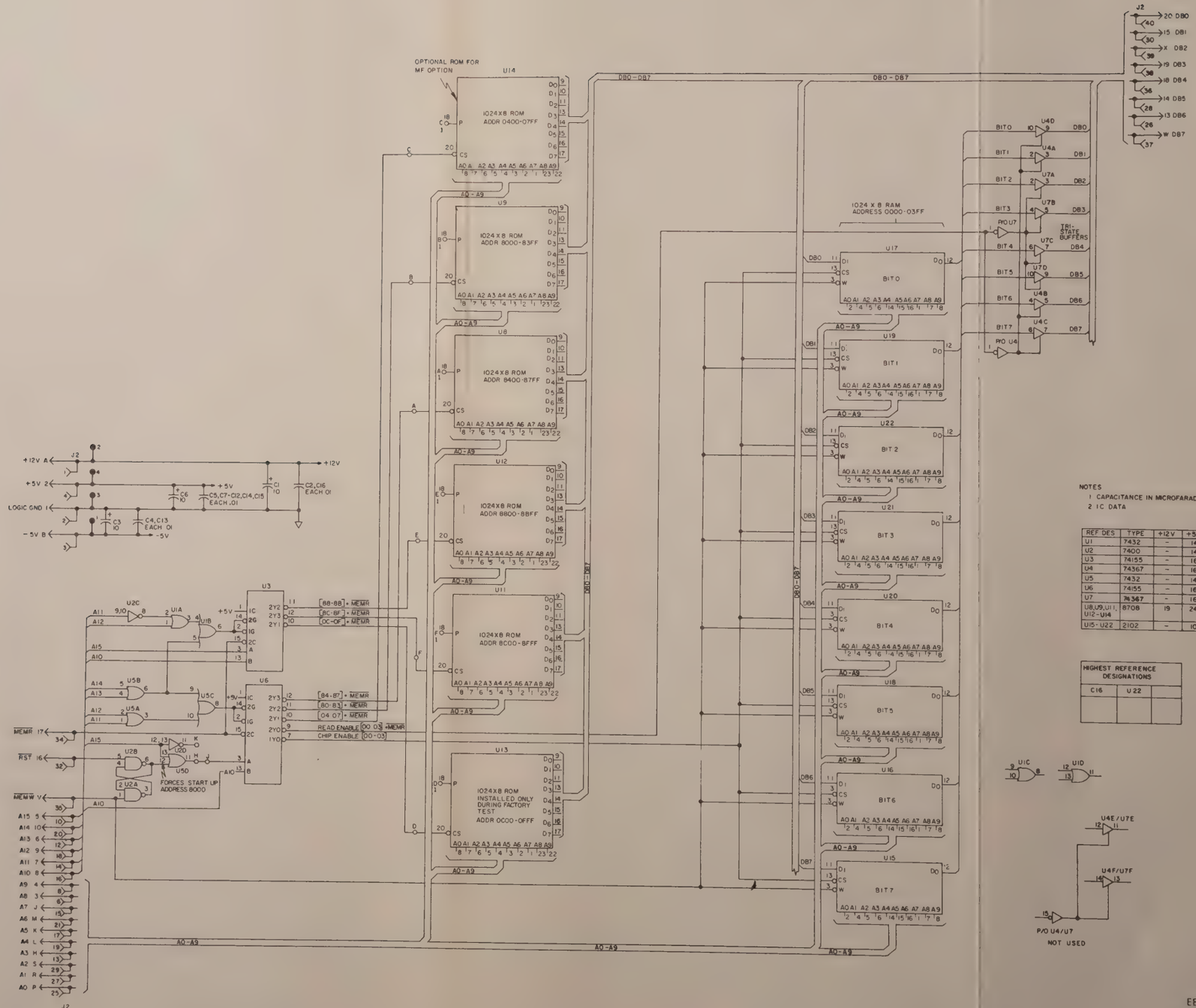


Figure 2—27. Memory Board Component Location Diagram.



NOTES
1 CAPACITANCE IN MICROFARADS
2 I.C. DATA

REF DES	TYPE	+12V	+5V	-5V	GND
U1	7432	-	14	-	7
U2	7400	-	14	-	7
U3	74155	-	16	-	8
U4	74367	-	16	-	8
U5	7432	-	14	-	7
U6	74155	-	16	-	8
U7	74367	-	16	-	8
U8,U9,U11, U12-U14	8708	19	24	21	12
U15-U22	2102	-	10	-	9

HIGHEST REFERENCE DESIGNATIONS		
C16	U22	

EE0041-13-341

Memory	
NE PART NO.	B0041-13-041
REF DESIG	A10
PC NO.	96703
CARD SLOT	10

Figure 2—28. Memory Board Schematic Diagram.

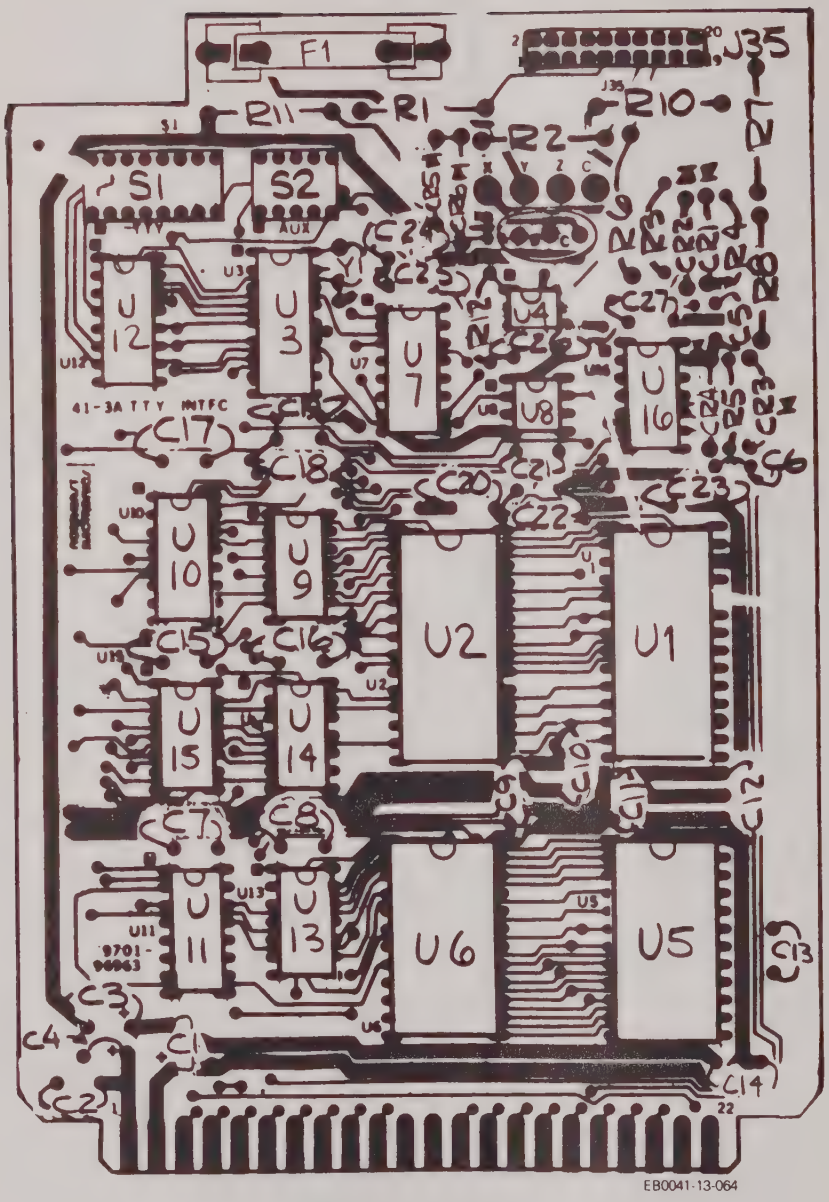


Figure 2—29. Optional TTY Interface Component Location Diagram.

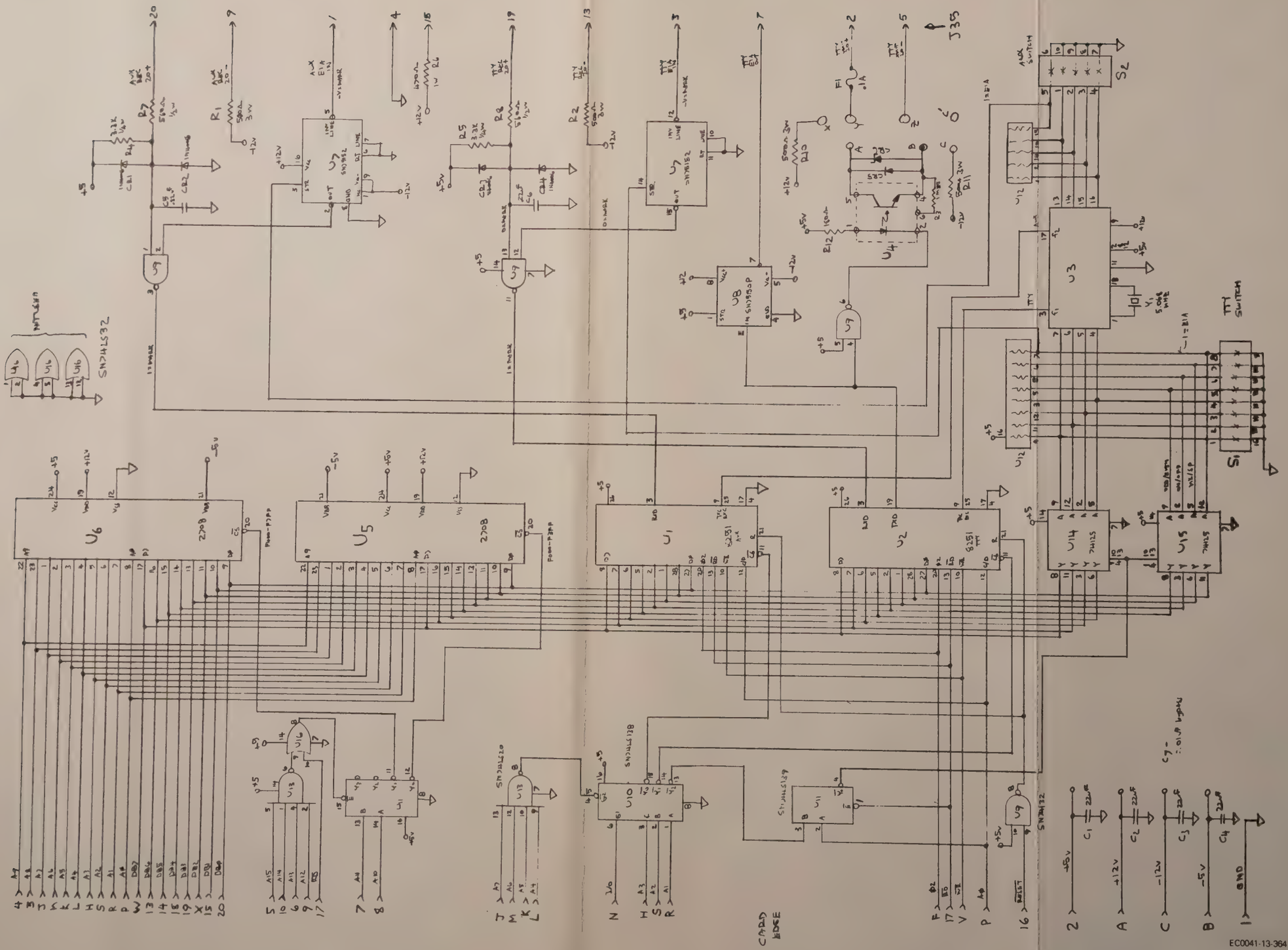


Figure 2—30. Optional TTY Interface Schematic Diagram.

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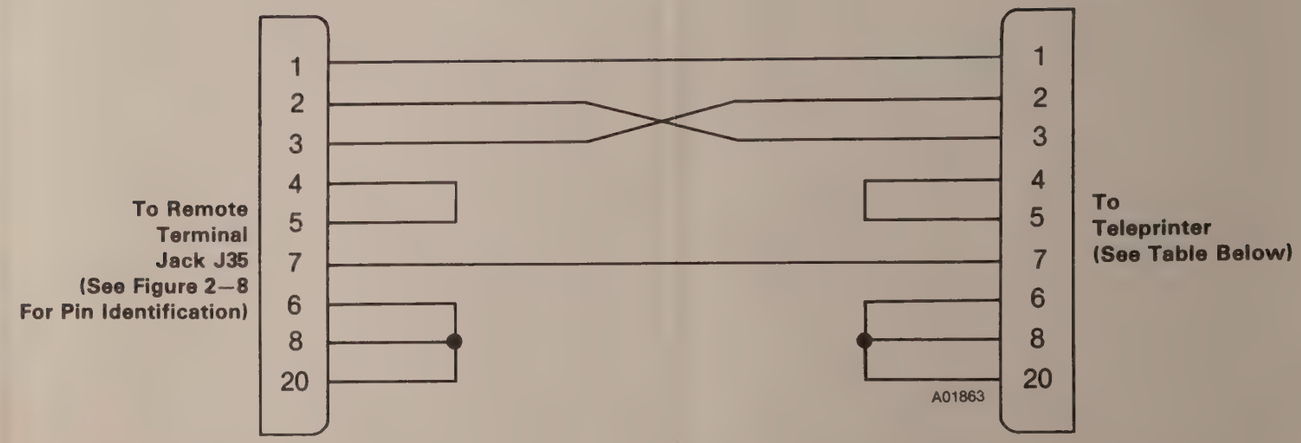


Pin Identification For Null Modem Cable Inserted In REMOTE TERMINAL Connector.

PIN	FUNCTION	EIA RS-232C SIGNAL NAME
1	Ground	Protective Ground
2	41-3A RS-232C output port	Transmitted Data
3	41-3A RS-232C input port	Received Data
4	Tied to pin 5	Request To Send
5	Tied to pin 4	Clear To Send
6	Tied to pins 8 and 20	Data Set Ready
7	Ground	Signal Ground
8	Tied to pins 6 and 20	Received Line Signal Detector
20	Tied to pins 6 and 8	Data Terminal Ready

Figure 2—31. Null Modem Cable Schematic Diagram (Part Of TTY Option).

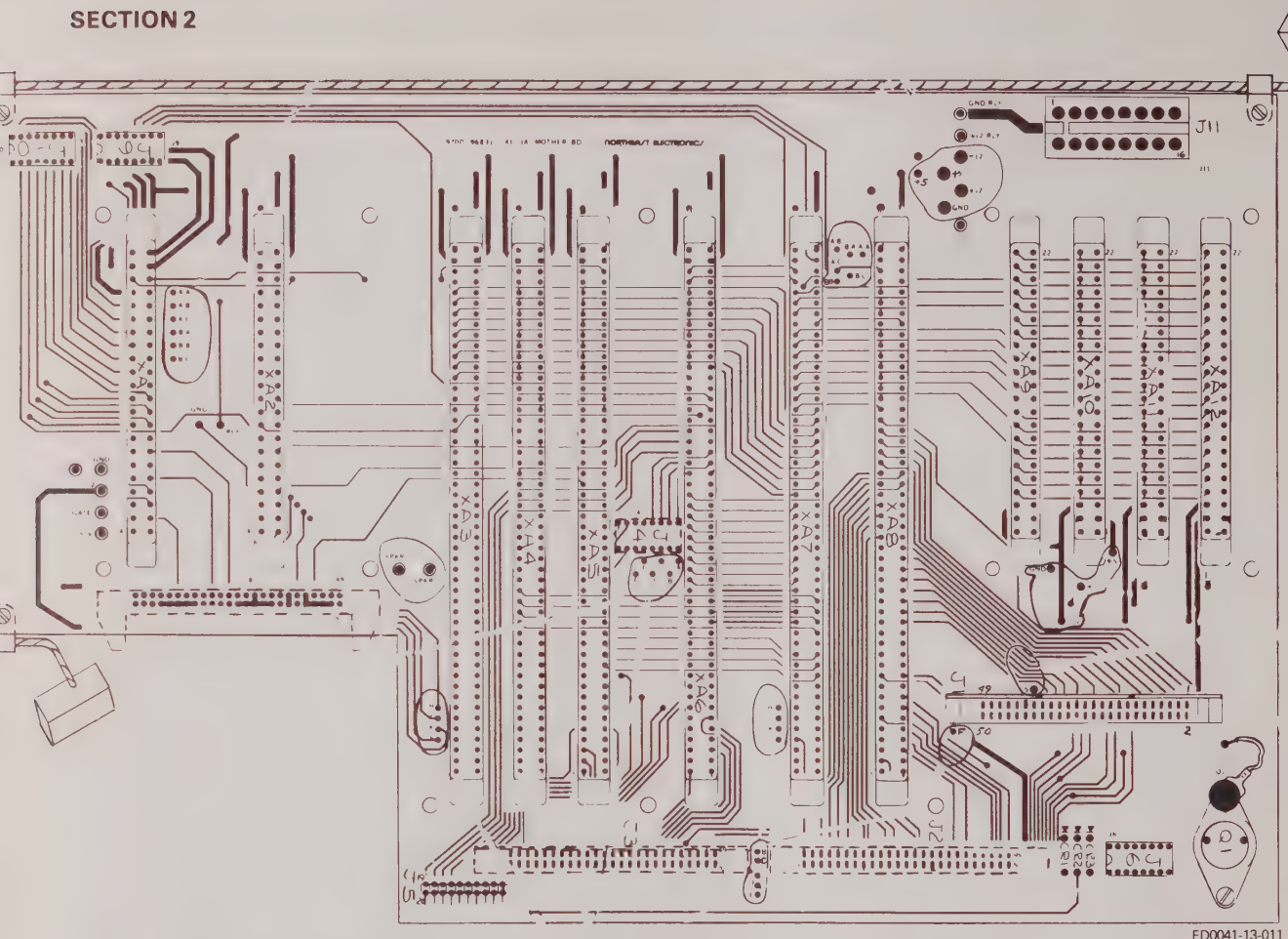


Figure 2—32. Mother Board Component Location Diagram.

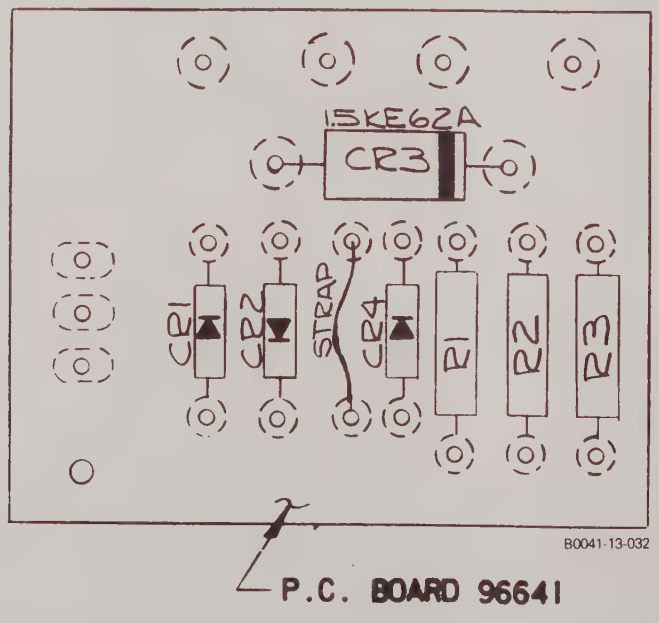
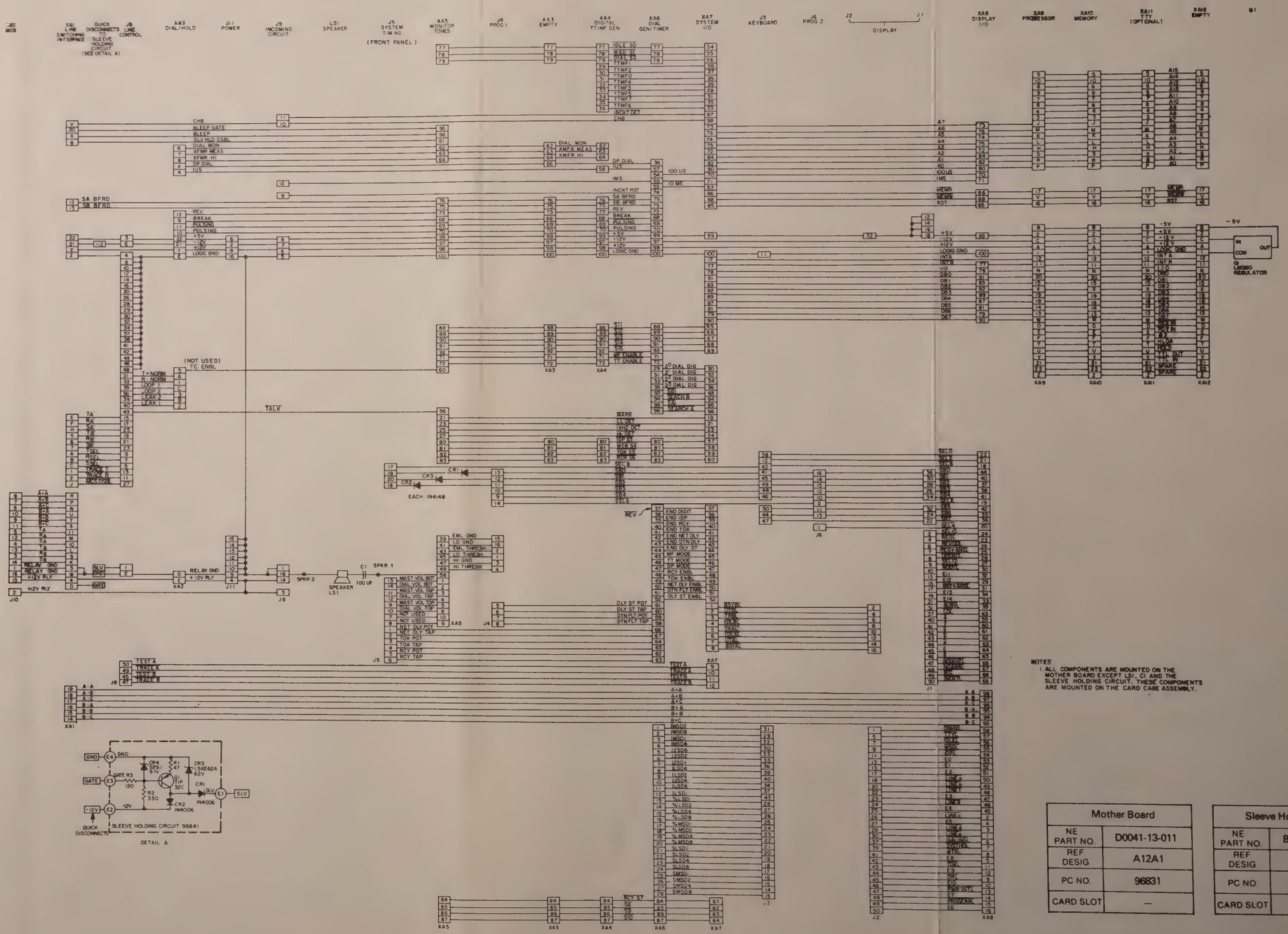


Figure 2—33. Sleeve Holding Circuit Component Location Diagram.



Mother Board	
NE PART NO.	D0041-13-011
REF DESIG	A12A1
PC NO.	96831
CARD SLOT	—

Sleeve Holding Ckt.	
NE PART NO.	B0041-13-033
REF DESIG	A12A2
PC NO.	96641
CARD SLOT	—

EE0041-13-311

Figure 2—34. Card Cage Assembly Schematic Diagram.

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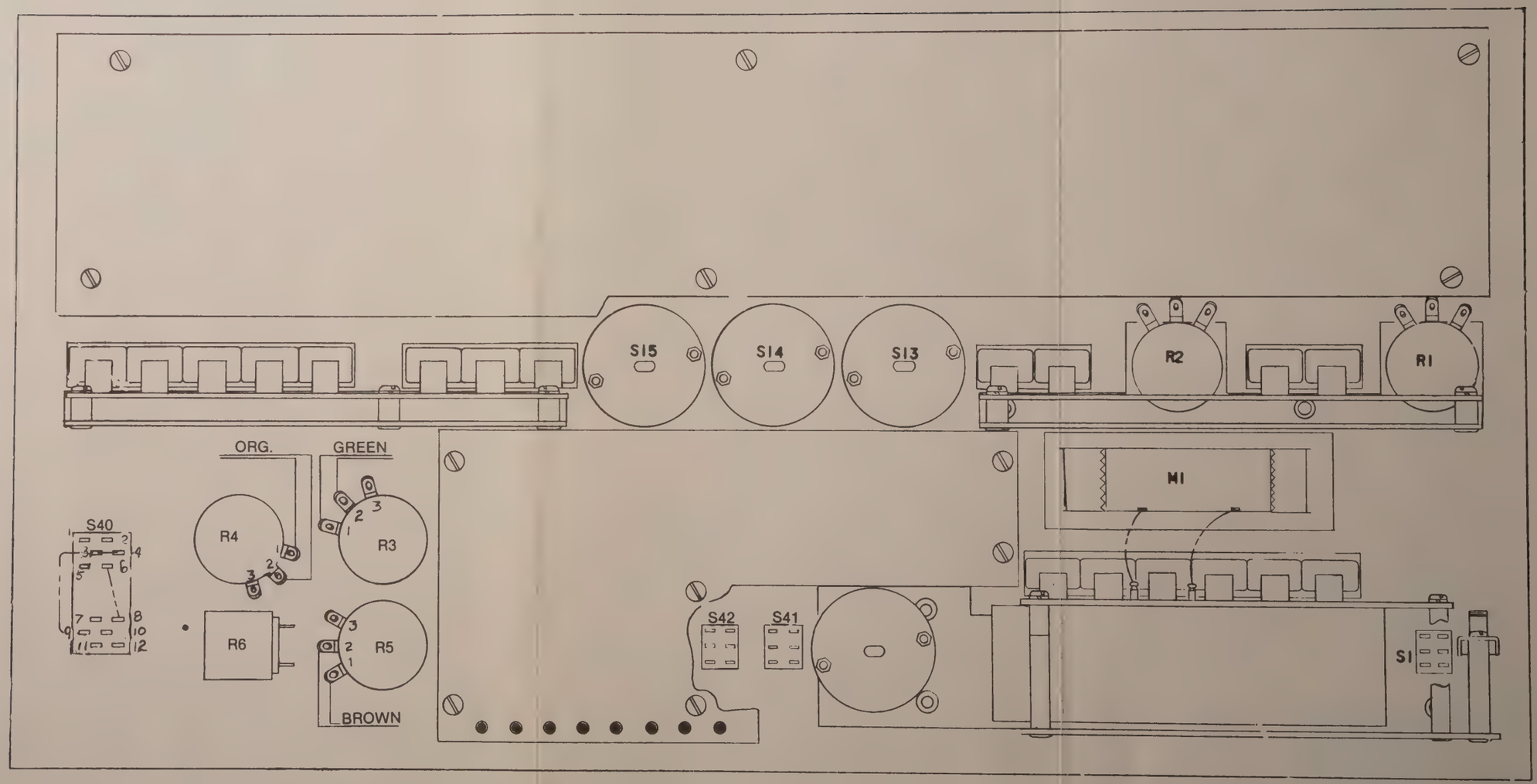


Figure 2–35. Front Panel Assembly Component Location Diagram.

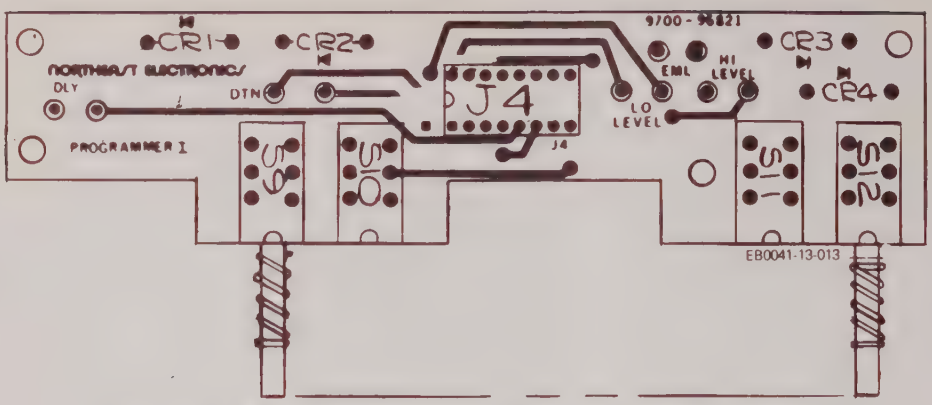


Figure 2—36. Programmer I Component Location Diagram.

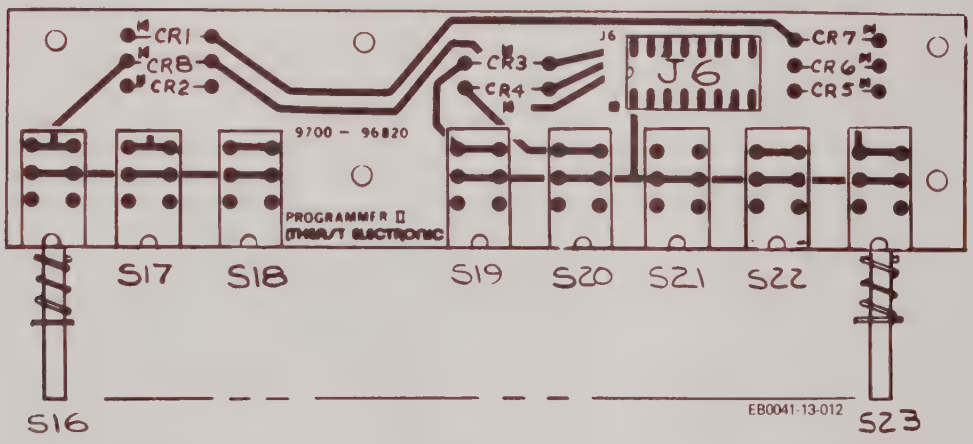


Figure 2—37. Programmer II Component Location Diagram.

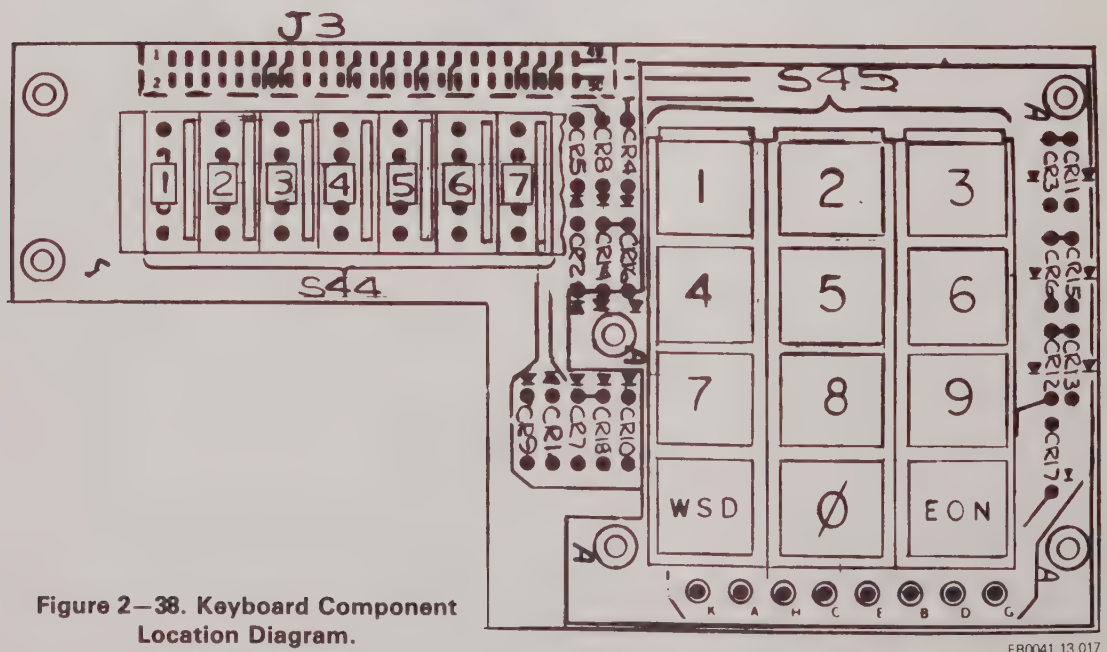
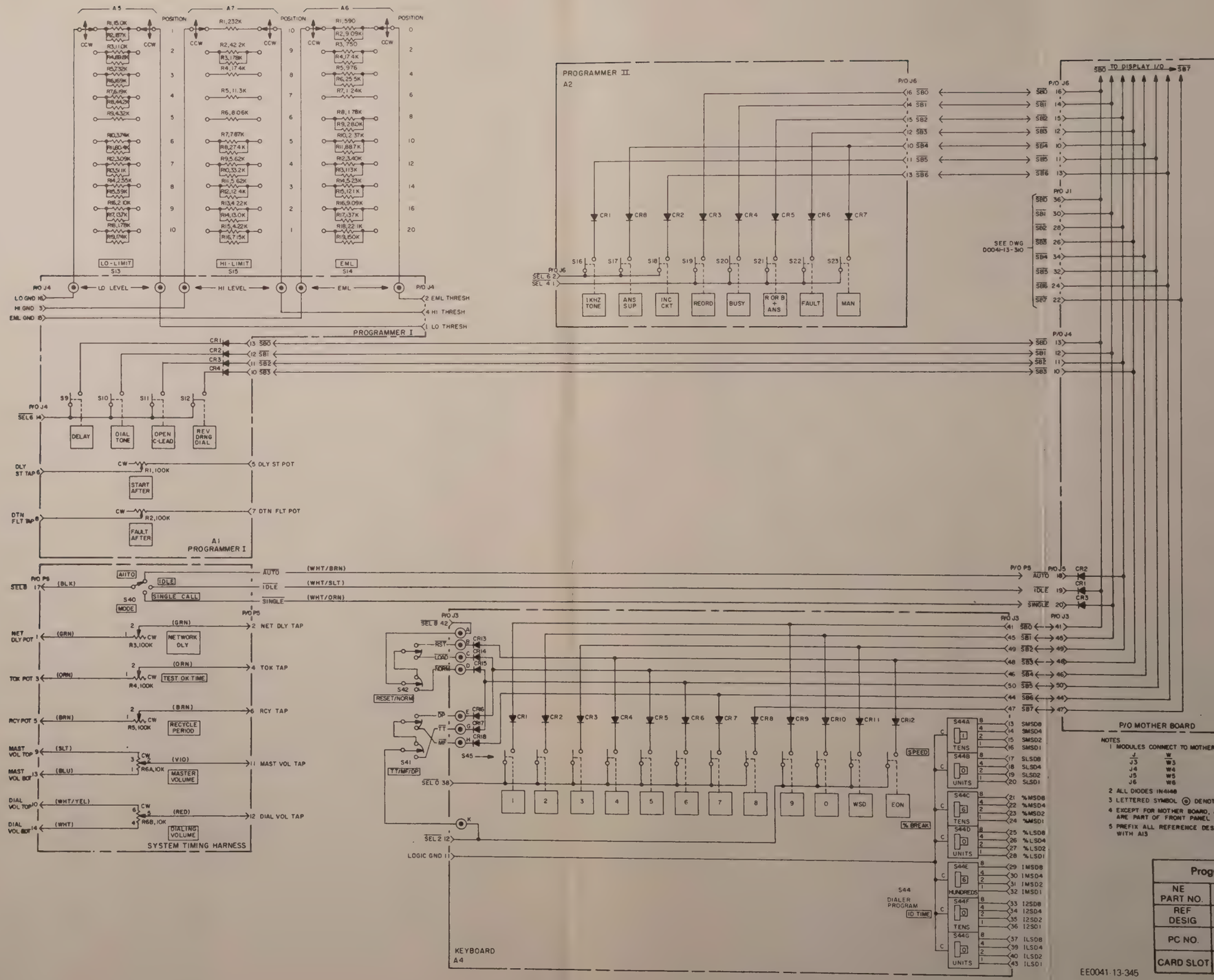


Figure 2—38. Keyboard Component Location Diagram.



NOTES
1 MODULES CONNECT TO MOTHERBOARD AS FOLLOWS

J	W
J3	W3
J4	W4
J5	W5
J6	W6

2 ALL DIODES IN4448
3 LETTERED SYMBOL ⓐ DENOTES QUICK-DISCONNECT POST
4 EXCEPT FOR MOTHER BOARD, ALL ASSEMBLIES ARE PART OF FRONT PANEL A13
5 PREFIX ALL REFERENCE DESIGNATIONS SHOWN WITH A13

EE0041-13-345

Programmer I	
NE PART NO.	B0041-13-013
REF DESIG	A13A1
PC NO.	96821
CARD SLOT	—

Programmer II	
NE PART NO.	B0041-13-012
REF DESIG	A13A2
PC NO.	96820
CARD SLOT	—

Keyboard	
NE PART NO.	B0041-13-017
REF DESIG	A13A4
PC NO.	96829
CARD SLOT	—

Figure 2—39. Front Panel Schematic Diagram.

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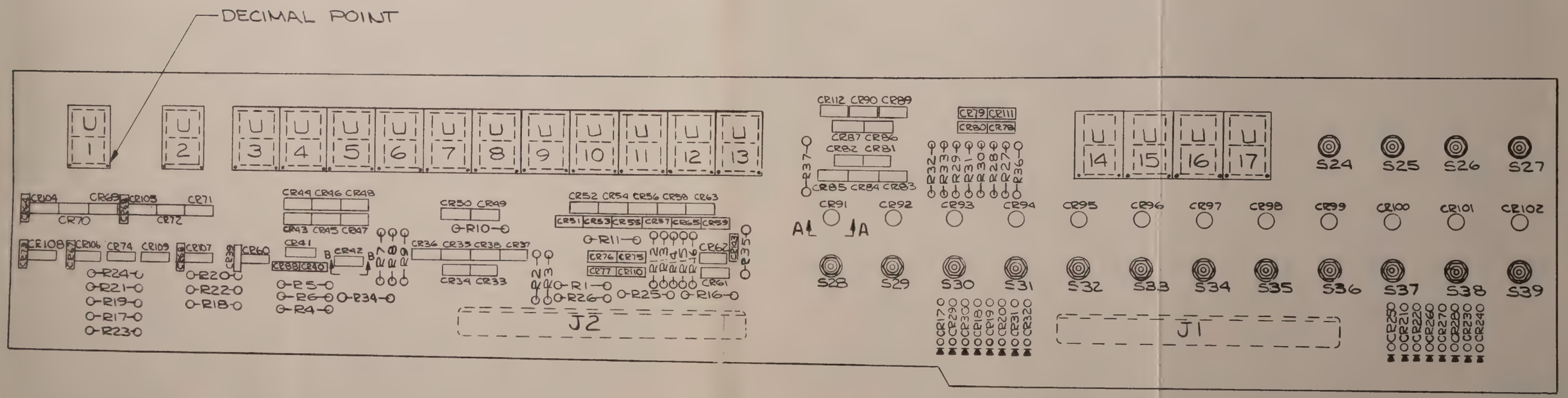
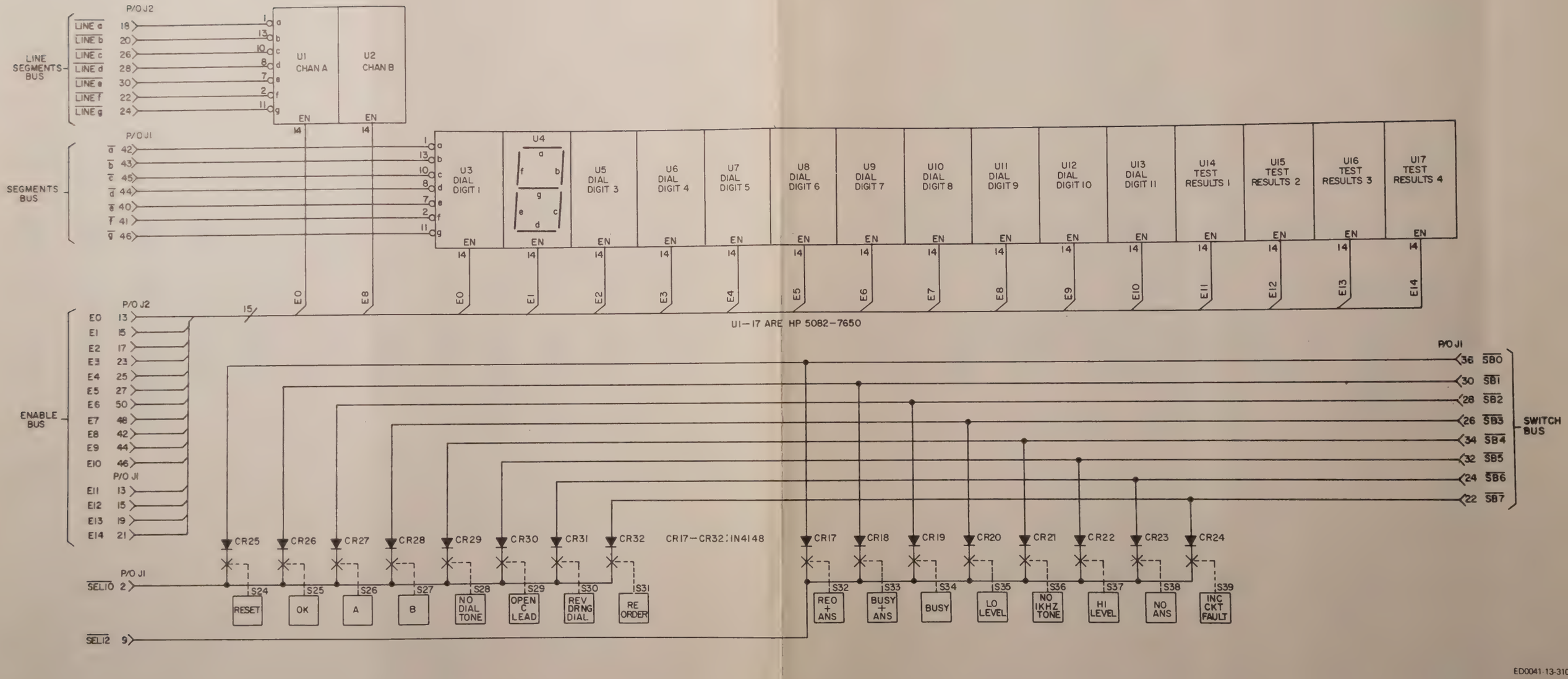


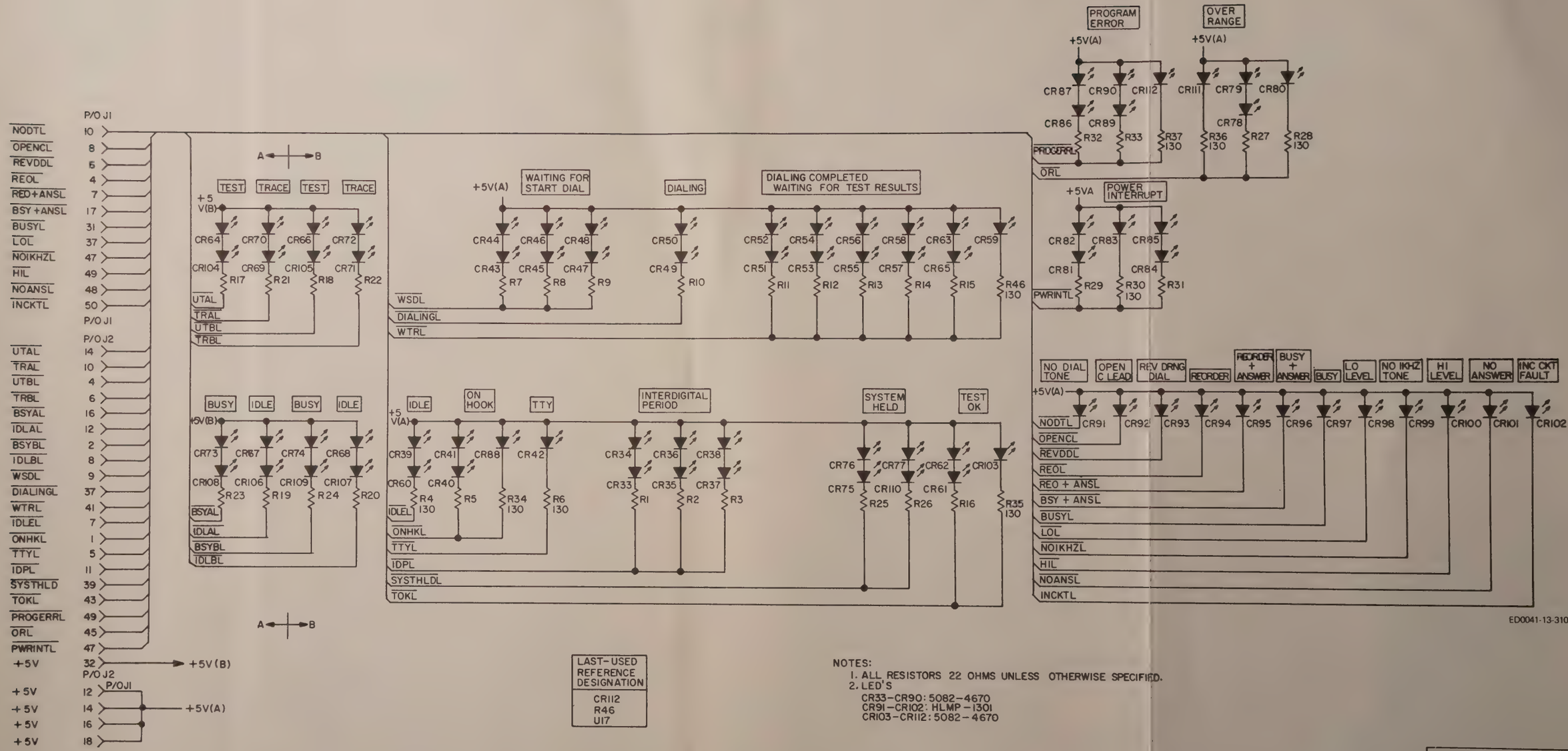
ED0041-13-010

Figure 2—40. Display Board Component Location Diagram.



ED0041-13-310

Figure 2—41. Display Board Schematic Diagram (Sheet 1 of 2).



ED0041-13-310

LAST-USED REFERENCE DESIGNATION
CR112
R46
U17

NOTES:
1. ALL RESISTORS 22 OHMS UNLESS OTHERWISE SPECIFIED.
2. LED'S
   CR33–CR90: 5082–4670
   CR91–CR102: HLMP–1301
   CR103–CR112: 5082–4670

Display Board	
NE PART NO.	D0041-13-010
REF DESIG	A13A3
PC NO.	96813
CARD SLOT	–

Figure 2–41. Display Board Schematic Diagram (Sheet 2 of 2).

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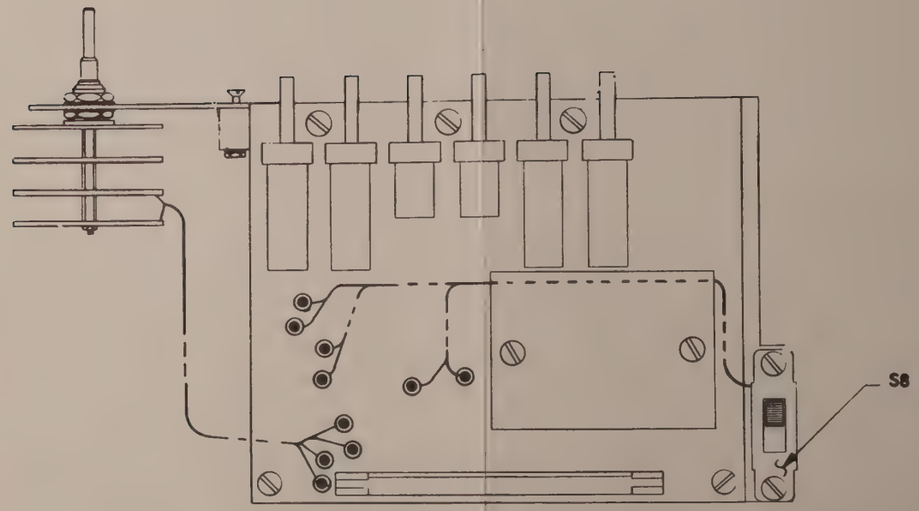


ED0041 13-048

Figure 2—42. Line Control Module Component Location Diagram.

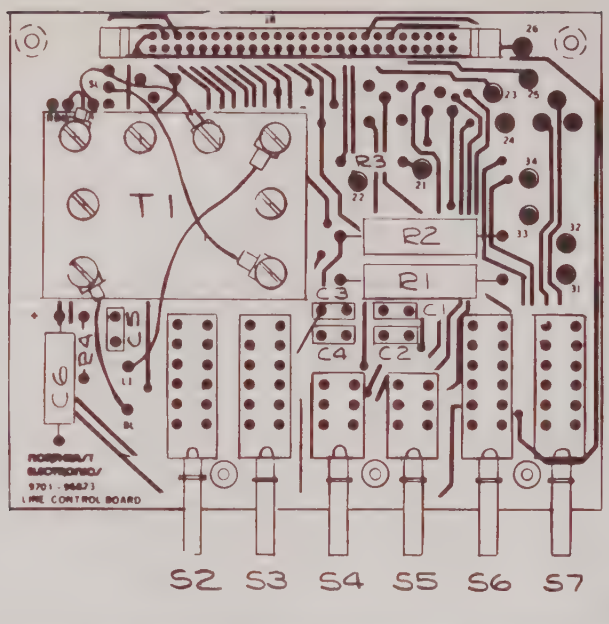


Figure 2—43. Line Control Board Component Location Diagram.

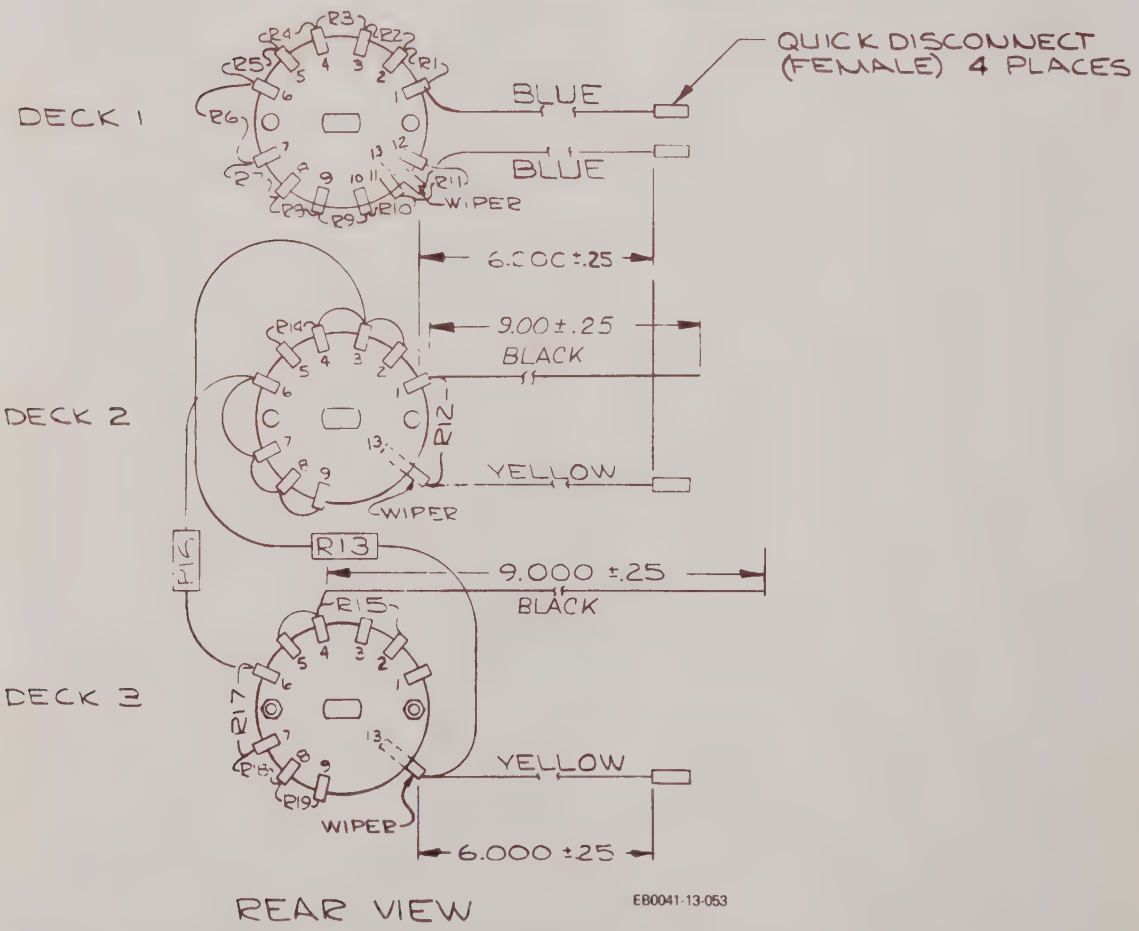
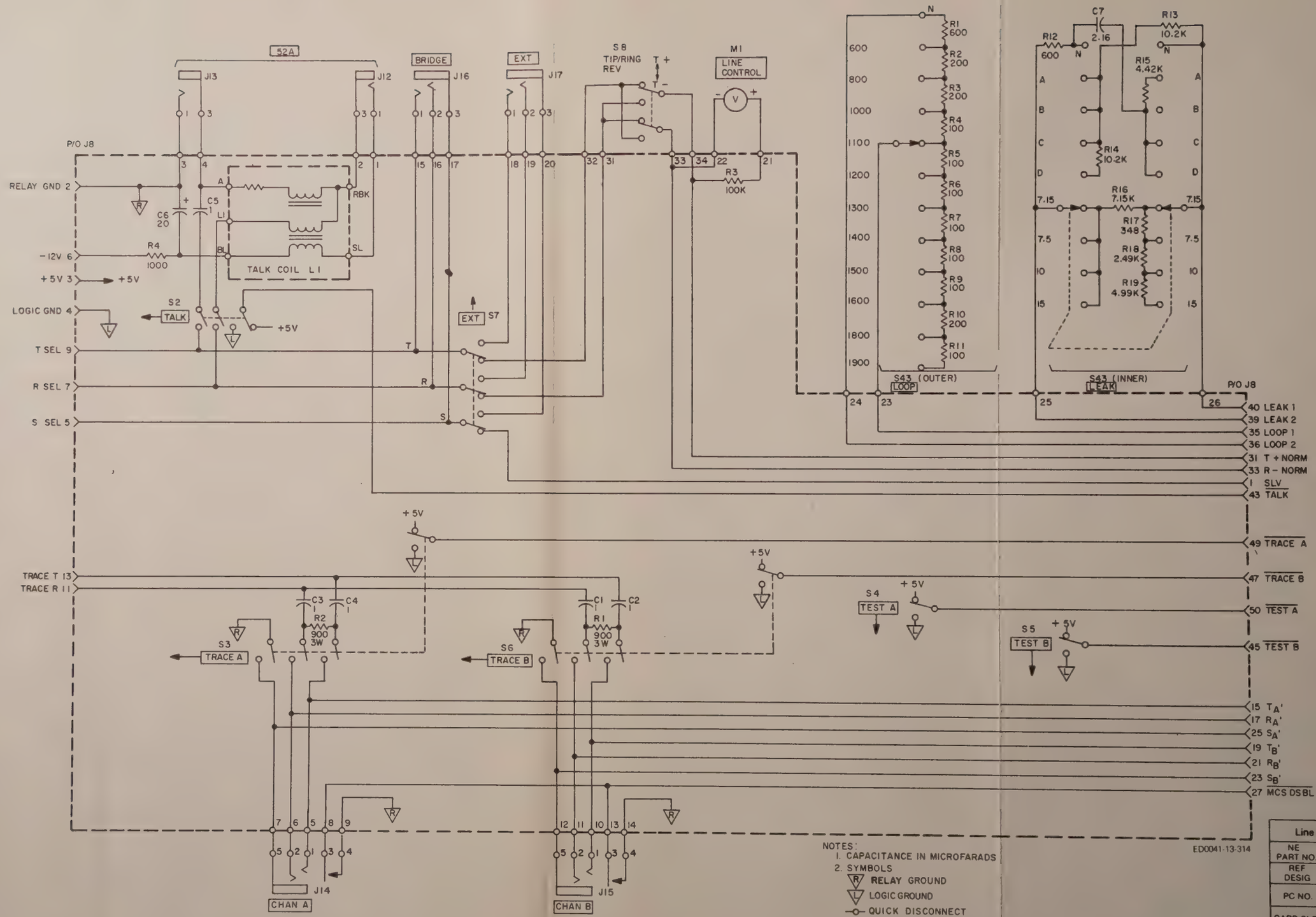


Figure 2—44. Loop And Leak Network Component Location Diagram.



NOTES:
1. CAPACITANCE IN MICROFARADS
2. SYMBOLS
   - R RELAY GROUND
   - LOGIC GROUND
   - QUICK DISCONNECT
3. W8 CONNECTS J8 TO J8 ON MOTHER BOARD

ED0041-13-314

Line Control Board	
NE PART NO.	B0041-13-014
REF DESIG	A13A8A1
PC NO.	98823
CARD SLOT	–

Figure 2–45. Line Control And Loop & Leak Schematic Diagram.

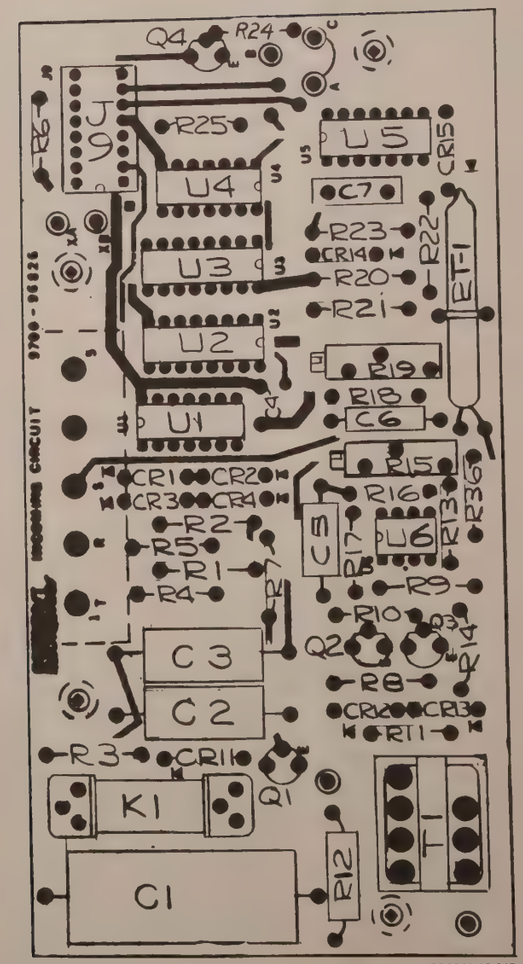
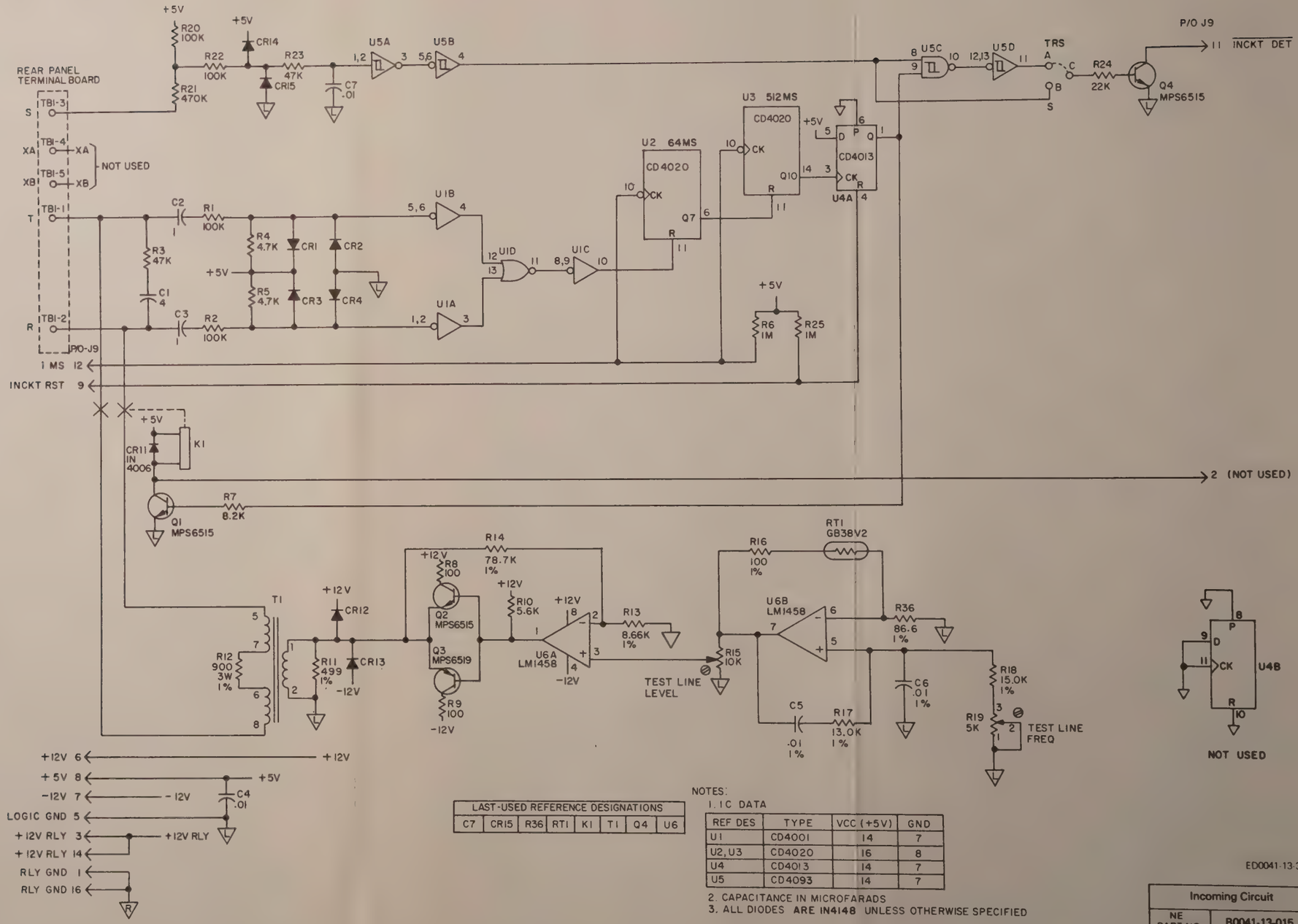


Figure 2—46. Incoming Circuit Component Location Diagram.



LAST-USED REFERENCE DESIGNATIONS							
C7	CR15	R36	RT1	K1	T1	Q4	U6

NOTES:
1. IC DATA

REF DES	TYPE	VCC (+5V)	GND
U1	CD4001	14	7
U2, U3	CD4020	16	8
U4	CD4013	14	7
U5	CD4093	14	7

2. CAPACITANCE IN MICROFARADS
3. ALL DIODES ARE IN4148 UNLESS OTHERWISE SPECIFIED

ED0041-13-315

Incoming Circuit	
NE PART NO.	B0041-13-015
REF DESIG	A14A1
PC NO.	96826
CARD SLOT	—

Figure 2–47. Incoming Circuit Schematic Diagram.

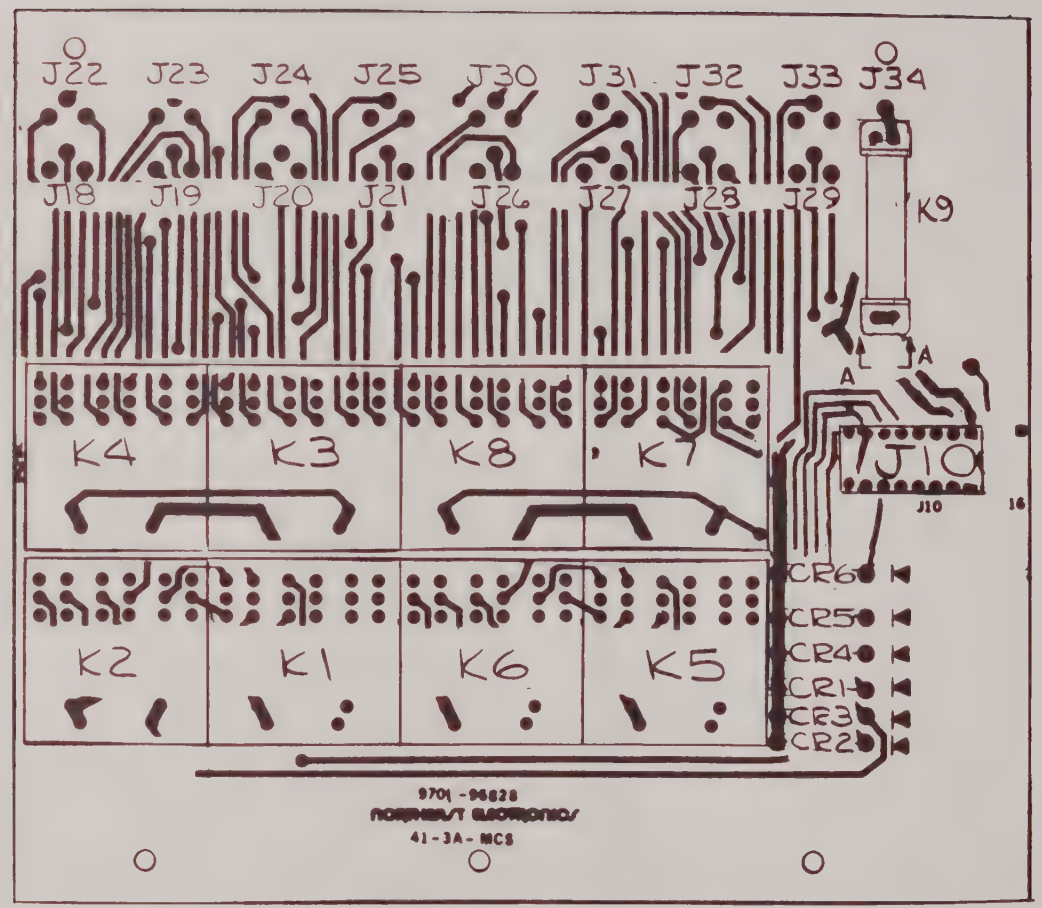
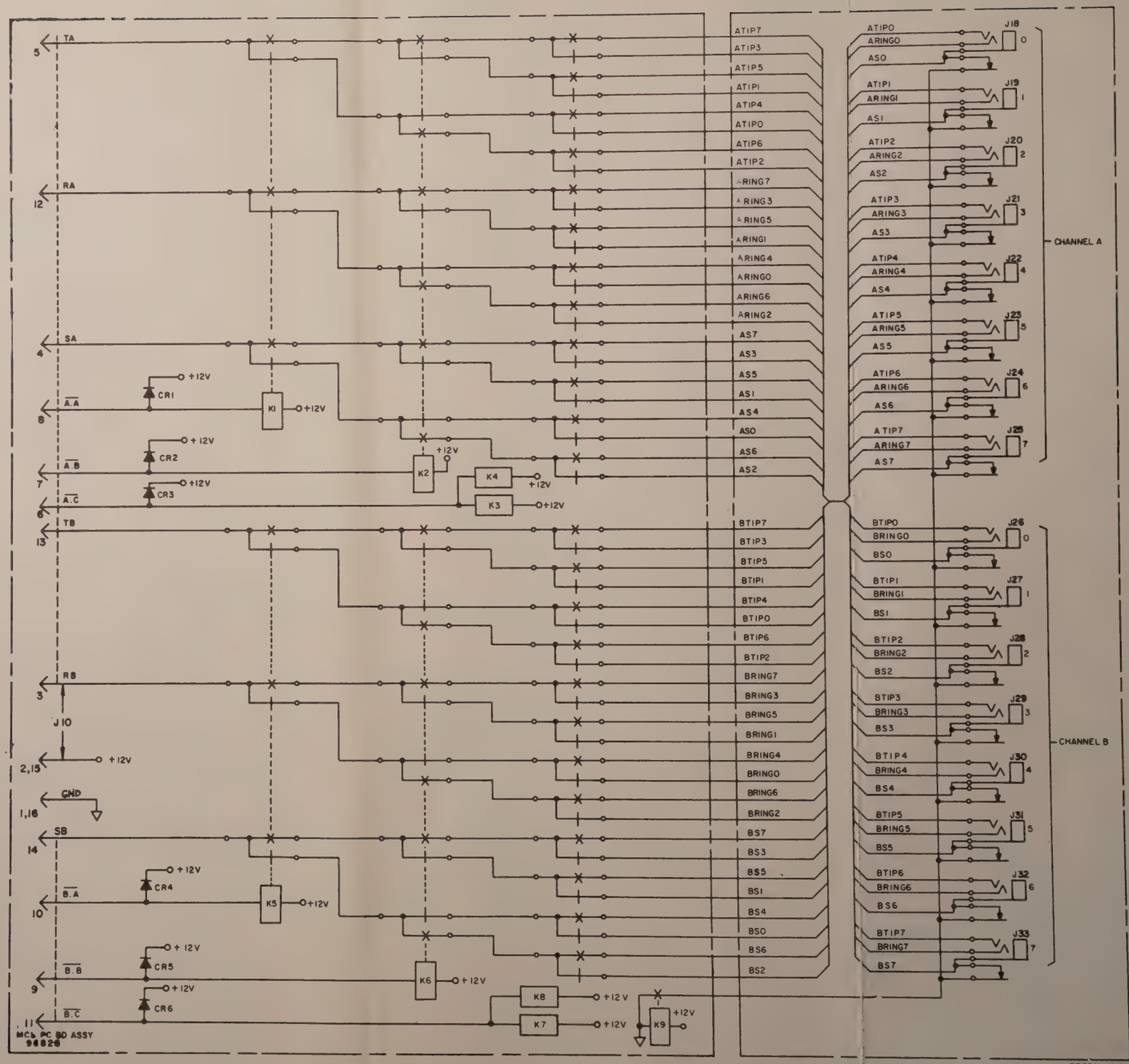
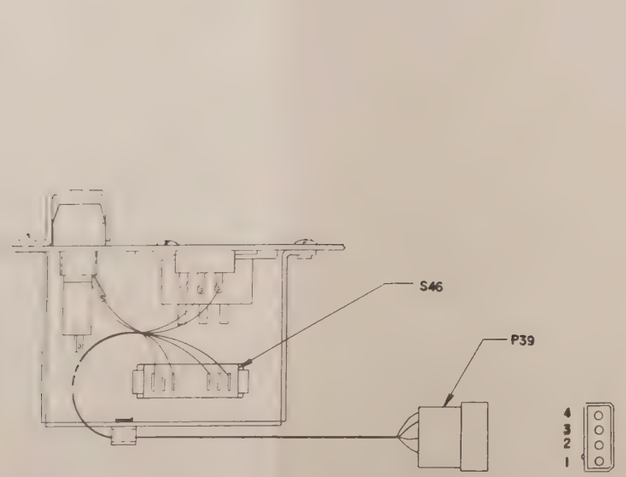


Figure 2—48. MCS Module Component Location Diagram.



MCS Module	
NE PART NO.	D0041-13-049
REF DESIG	A14A2
PC NO.	96828
CARD SLOT	—

Figure 2–49. MCS Module Schematic Diagram.



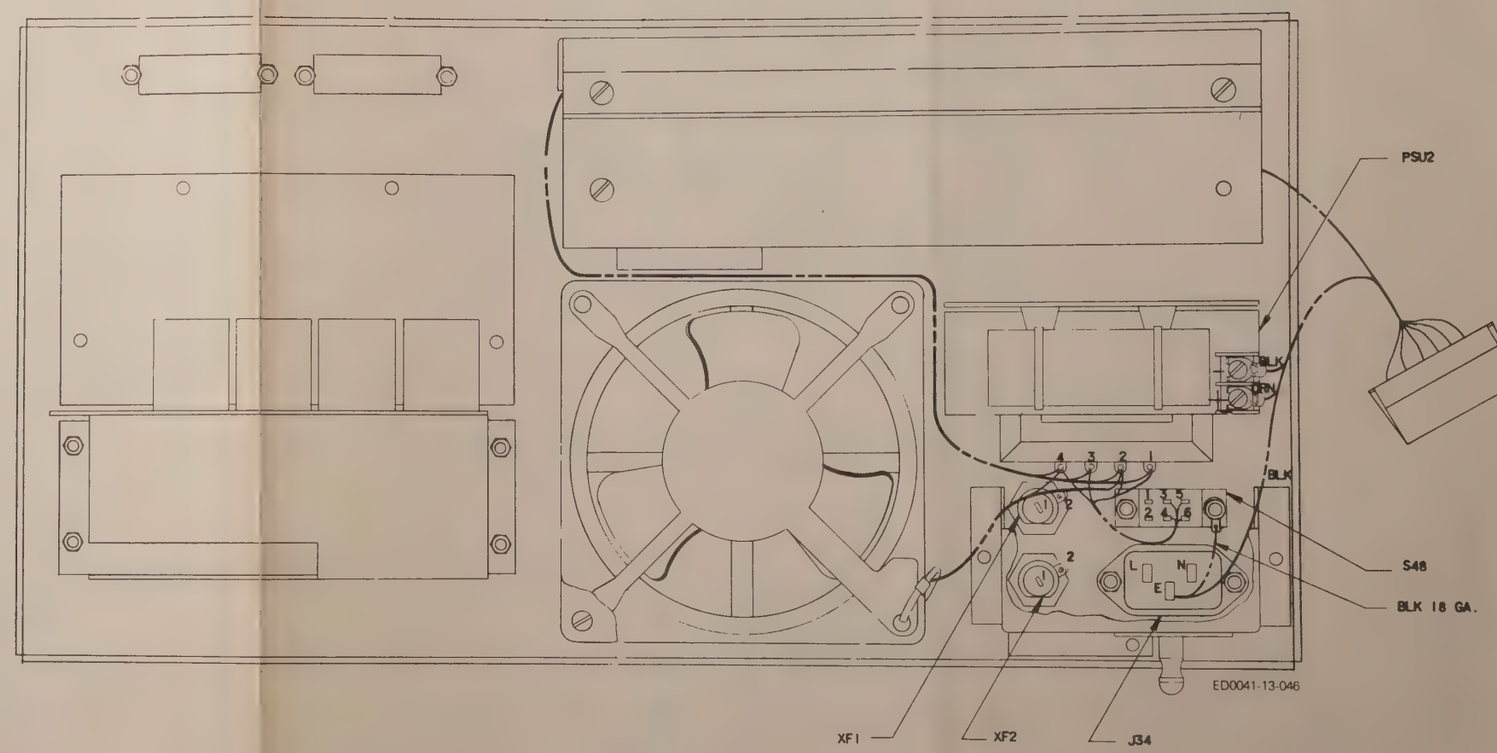
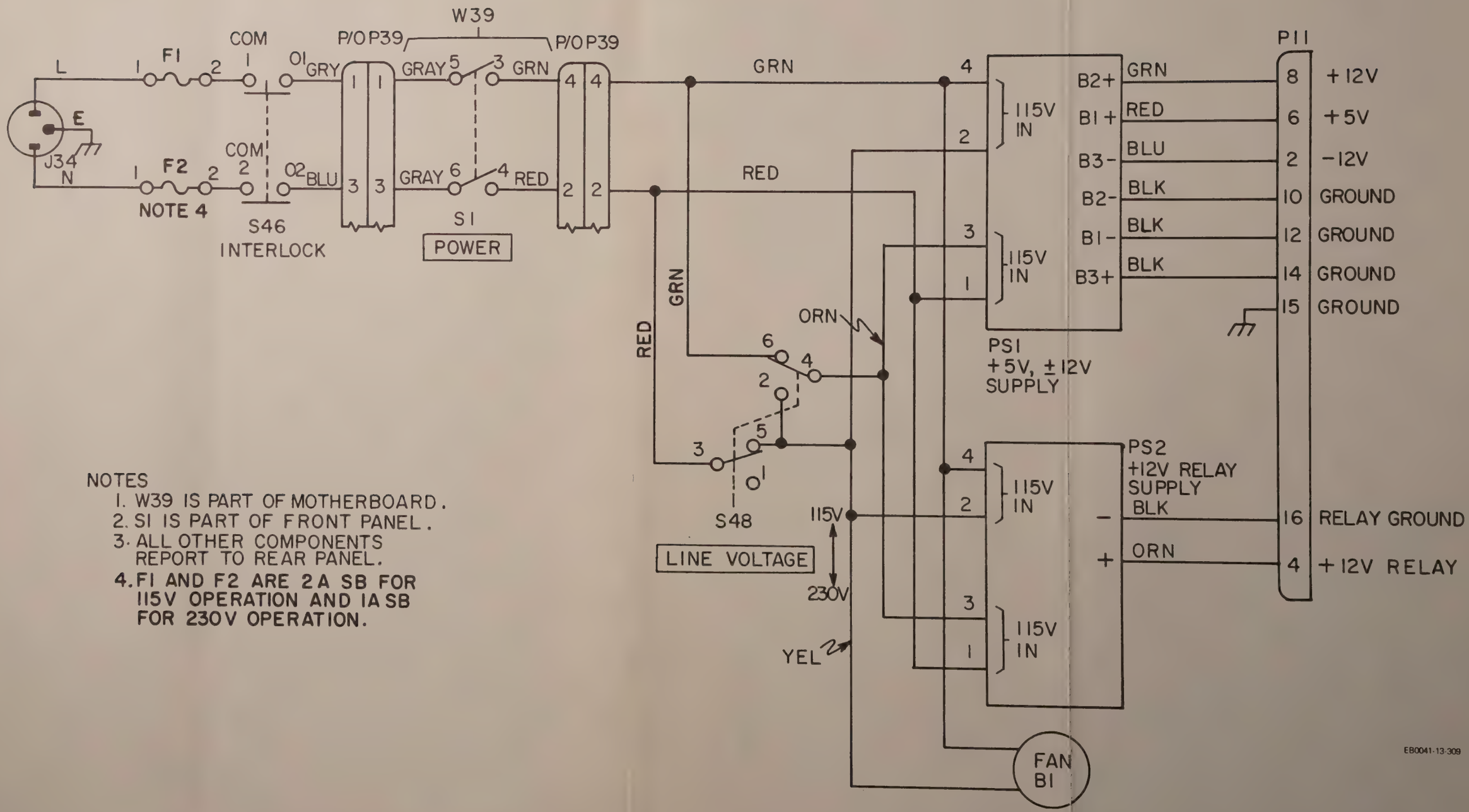


Figure 2—50. Rear Panel Assembly Component Location Diagram.



NOTES

1. W39 IS PART OF MOTHERBOARD.
2. S1 IS PART OF FRONT PANEL.
3. ALL OTHER COMPONENTS REPORT TO REAR PANEL.
4. F1 AND F2 ARE 2A SB FOR 115V OPERATION AND 1A SB FOR 230V OPERATION.

EB0041-13-309

Figure 2–51. Power Wiring Schematic Diagram.

SECTION 3

ELECTRONIC PARTS LISTS

3.1 Tables 3—1 through 3—29 list the electronic parts for the TTS 41-3A Service Analyzer. The component location diagrams contained in Section 2 show reference designations and locations of all electronic components.

Table 3—1. Overall Assembly Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
A9	BMSC E/W ACIA						A004113078
A1	PC ASSY 96815 LINE SW						A004113018
A2	PC ASSY 96814 DIAL./HOLD						A004113019
A4	PC ASSY 96825 TTMF BD						A004113020
A5	PC ASSY 96830 ANALOG DET.						A004113021
A6	PC ASSY 96824 DIAL/TIMER						A004113022
A7	PC ASSY 96818 SYSTEM I/O						A004113023
A8	PC ASSY 96819 FRT PNL I/O						A004113024
A10	41-3A MEMORY CARD ASSY						A004113041
P1-2	FLAT CABLE (50 LONG)						A004113034
P3	FLAT CABLE (50 SHORT)						A004113035
P4	FLAT CABLE (16 LONG)						A004113036
P6	FLAT CABLE (16 MEDIUM)						A004113037
P8	FLAT CABLE (50 SHORT)						A004113035
P9	FLAT CABLE (16 MEDIUM)						A004113037
P10	FLAT CABLE (16 SHORT)						A004113038
A11	TTY INTERFACE (OPTIONAL)						A004113064
A12	CARD CAGE ASSY						A004113047
A13	FRONT PANEL ASSY						A004113045
A14	REAR PANEL ASSY						A004113046

Table 3—2. Line Switching Interface B0041-13-018 A1 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1	.33UF		10%	100V	SPRAGUE	225P33491XD3	320003340
C2	.01UF		10%	100V	SPRAGUE	225P10391WD3	320001030
C4-6	.01UF		10%	100V	SPRAGUE	225P10391WD3	320001030
C7-9	22UF	B	10%	15V	SPRAGUE	196D226X9015KA1	310002263
CR1-2	D041	1A	SI	800V	EDAL	1N4006	560040060
CR3-6	D035	4NS 10MA	SI	50UA	FAIRCHILD	IN4148	560041480
CR7-8	D035	4NS 10MA	SI	50UA	FAIRCHILD	IN4148	560041480
K1-2	130-			12V	NIPPON	MR11N53	600601300
Q1	TO-92	350MW TA	NPN	25V	MOTOROLA	MPS6515	550065150
Q4	TO-92	350MW TA	NPN	25V	MOTOROLA	MPS6515	550065150
Q5	TO5	7W TA	PNP	65V	RCA	2N4036	552040360
Q6-11	TO-92	350MW TA	NPN	25V	MOTOROLA	MPS6515	550065150
Q12-17	TO-5	1W TA	NPN	65V	RCA	2N2102	550021020
R1	100K	1/2W	10%		AB	TYPE EB	200201046
R7-12	22K	1/4W	10%		AB	TYPE CB	200102236
R13-14	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R15	22K	1/4W	10%		AB	TYPE CB	200102236
R16	2.2K	1/4W	10%		AB	TYPE CB	200102226
R20	3.3M	1/4W	10%		AB	TYPE CB	200103356
R21	330K	1/4W	10%		AB	TYPE CB	200103346
R22	390K	1/4W	10%		AB	TYPE CB	200103946
R23	39K	1/4W	10%		AB	TYPE CB	200103936
R26	10K	.75W	10%		HELIPOT	89PR10K	232501030
R27-28	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R29	100K	1/4W	10%		AB	TYPE CB	200101046
R30-31	47K	1/2W	10%		AB	TYPE EB	200204736
R32	100K	1/2W	10%		AB	TYPE EB	200201046
R33	47K	1/2W	10%		AB	TYPE EB	200204736
R35-37	47K	1/2W	10%		AB	TYPE EB	200204736
R38	560-	1/2W	10%		AB	TYPE EB	200205616
R39	300-	3W	5%		W LEONARD	TYPE 3X	210303015
T1	XFMR,PC,P600/S600				MICROTRAN	MT1-PC	400101300
U1	14 DIP-P	UB		CMOS	RCA	CD4001A	510014001
U2	8PDIL				NAT. SEMI	LM741CN	500007412
U3	14 DIP-P	UB		CMOS	RCA	CD4001A	510014001

Table 3—3. Dialing/Hold B0041-13-019 A2 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
A7	L1/CONTROL						A004113072
C1	2UF		10%	100V	F-DYNE	MPC12-2.0-100-10	321802050
C2	.033UF		10%	100V	SPRAGUE	225P33391WD3	320003330
C3	.047UF		10%	100V	SPRAGUE	225P47391WD3	320004730
C5	68PF	DB N3300	10%	1KV	CENTRALAB	DD-680	330006800
C6	.033UF		10%	100V	SPRAGUE	225P33391WD3	320003330
C7-8	560PF	DB Z5R	10%	1KV	CENTRALAB	DD-561	330005610
CR1-7	D041	1A SI		800V	EDAL	1N4006	560040060
CR8-9	D035	4NS 10MA SI		50UA	FAIRCHILD	IN4148	560041480
CR10	D07	.25W	5%	6.2V	DICKSON	1N823	563008230
CR11-12	D07	250MW	10%	8.75	T.I.	1N764	562007640
CR13-14	D041	1A SI		800V	EDAL	1N4006	560040060
CR15-16	TRANZORB				GEN.SEMI.	1.5KE150	565000004
CR18	D041	1A SI		800V	EDAL	1N4006	560040060
F1		.5A		250V	BUSSMAN	MDL	863101900
K1	RELAY,REED,PC2AMUSTOP			4V	MIDTEX	172-124BA1	604103100
K3	RELAY REED				D.RANDALL	377-598	604105601
Q1-3	TO-92	350MW TA NPN		25V	MOTOROLA	MPS6515	550065150
Q5-6	TO-92	350MW TA NPN		25V	MOTOROLA	MPS6515	550065150
Q7	TO-92	350MW TA NPN		40V	MOTOROLA	2N3903	550039030
Q8	TO-5	1W TA NPN		350V	RCA	2N3439	550034390
Q9	TO39/FLG	10W TC NPN		350V	RCA	2N4063	550004063
R1-2	47K	1/4W	10%		AB	TYPE CB	200104736
R3	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R4	10K	.75W	10%		HELIPOT	89PR10K	232501030
R5	1K	.75W	10%		HELIPOT	89PR1K	232501020
R6	150-	3W	5%		W.LEONARD	TYPE 3X	210301510
R7	470K	1/2W	10%		AB	TYPE EB	200204745
R10	1M	1/4W	10%		AB	TYPE CB	200101056
R11	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R12	330-	1/2W	10%		AB	TYPE EB	200203316
R13	1M	1/4W	10%		AB	TYPE CB	200101056
R14	1210-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212111
R15	909-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220290901
R16	3320-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220233211
R19	5.6K	1/4W	10%		AB	TYPE CB	200105626
R21	390-	1/4W	10%		AB	TYPE CB	200103916
R22	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R23	47-	1/4W	10%		AB	TYPE CB	200104706
R25	1K	.75W	10%		HELIPOT	89PR1K	232501020
R26	1M	1/4W	10%		AB	TYPE CB	200101056
R27	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R30	10-	1/4W	10%		AB	TYPE CB	200101006
T1	XFMR,PC,P600/S600				MICROTRAN	MT1-PC	400101300
T2	16DILP				ARTTED	AC8326	440200100
U1-2	6 DIP	125MA		55V	MONSANTO	MCA2-55	515000100
U3	16DIP-P	B		CMOS	RCA	CD4049	510004049
XF1	3AG				LITTELFUSE	102069	863300300

Table 3—4. L1 Control B0041-13-072 A2A7 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
CR17	D041 1A SI			800V	EDAL	1N4006	560040060
CR19	VARISTOR, MET OXIDE				G.E.	V150ZA1	565500150
K2	RELAY, MERC. REED				FIFTH DIM.	LC2R-1700-05	602500400
L1	HOLD COIL				N.T.I.	A024-0145	450200202
Q10	TO-92 350MW TA PNP			40V	MOTOROLA	MPS6518	550065180
Q11	TO-92 625MW TA PNP			80V	MOTOROLA	MPS A-56	552000560
R17	47K ¼W	10%			AB	TYPE CB	200104736
R18	2.2K ¼W	10%			AB	TYPE CB	200102226

Table 3—5. Digital TT/MF Generator C0041-13-020 A4 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-4	.J10F		1%	100V	ELECTROCBE	730B1B103F	32260103O
C5	22UF	B	10%	15V	SPRAGUE	196D226X9015KA1	310802263
C6-15	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C16	1.0UF MD	Y5V	20%	50V	ERIE	8131-050-651-105M	330801050
CR1	A1	400MW	5%	5.1V	DICKSON	1N751A	562007511
CR2	D041	1A SI		800V	EDAL	1N4006	560040060
K1	RELAY,1A-PC				MIDTEX	172112B00	604103500
Q1	TO92 350MW TC PNP			25V	MOTOROLA	MPS6519	552065190
R1-26	5.6K	1/4W	10%		AB	TYPE CB	200105626
R27	100K	1/4W	10%		AB	TYPE CB	200101046
R28	470-	1/4W	10%		AB	TYPE CB	200104716
R29	10K	1/4W	10%		2	00 A4101000015R71-7	200101036
R30	261K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226131
R31	71.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220271521
R32	38.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220238321
R33	27.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227421
R34	24.98K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220224921
R35	27.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227421
R36	38.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220238321
R37	71.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220271521
R38-39	261K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226131
R40	71.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220271521
R41	38.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220238321
R42	27.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227421
R43	24.98K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220224921
R44	27.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227421
R45	38.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220238321
R46	71.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220271521
R47	261K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226131
R48	27.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227421
R49-57	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R58	2.26K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222611
R59	8.06K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220280611
R60	3400-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234011
R61	3320-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220233211
R62	8.06K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220280611
R63	10K	.75W	10%		HELIPOT	89PR10K	232501030
U1	CT2.00 ROM						A004113051
U2	CT1.03 ROM						A004113050
U3-6	16 DIP-P	B		CMOS	MOTOROLA	MC14526	510004526
U7-8	16DIP-P	B		CMOS	RCA	CD4017	510004017
U9	14 DIP-P	B/UB		CMOS	MOTOROLA	MC14000	510004000
U10	16DIP-P	B		CMOS	RCA	CD4050	510004050
U11-14	8PD1L	80MW		180V	NAT.SEMI	LM1458N	500001458

Table 3—6. Monitor Tones Detector C0041-13-021 A5 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-4	1.0UF	MD Y5V	20%	50V	ERIE	8131-050-651-105M	330801050
C5-7	.47UF	MD Y5V	20%	50V	ERIE	8131-050-651-474M	330804740
C8-9	.01UF	00		50V	CENTRALAB	CK-103	330701030
C10-11	.1UF	MC Y5V	20%	50V	ERIE	8121-050-651-104M	330801040
C12	1.0UF	MD Y5V	20%	50V	ERIE	8131-050-651-105M	330801050
C13-16	.01UF		1%	100V	F-DYNE	PS11-01-100-1	321501031
C17	.47UF	MD Y5V	20%	50V	ERIE	8131-050-651-474M	330804740
C18	.01UF	00		50V	CENTRALAB	CK-103	330701030
C19-23	.05 UF		5%	100V	ELECTROCBE	230B1B503J	322850312
C24	.068 UF		5%	100V	ELECTROCBE	230B1B683J	322868312
C25	.18 UF		5%	100V	ELECTROCBE	230B1B184J	322818412
C26	.0027 UF		5%	400V	ELECTROCBE	230B1E272J	322827242
C27	.22 UF		5%	100V	ELECTROCBE	230B1B224J	322822412
C28		** NO FIXFLE **					322810162
C28	.001 UF		5%	600V	ELECTROCBE	230B1F102J	322810262
C29	.01UF		10%	100V	SPRAGUE	225P10391WD3	320001030
C32-34	22UF	B	10%	15V	SPRAGUE	196D226X9015KA1	310802263
C35	.01UF	00		50V	CENTRALAB	CK-103	330701030
C36-37	1.0UF	MD Y5V	20%	50V	ERIE	8131-050-651-105M	330801050
C38	.1UF	MC Y5V	20%	50V	ERIE	8121-050-651-104M	330801040
CR1-19	D035	4NS 10MA	SI	50UA	FAIRCHILD	IN4148	560041480
CR22-23	D035	4NS 10MA	SI	50UA	FAIRCHILD	IN4148	560041480
CR24-25	D07	.25W	5%	6.2V	DICKSON	1N823	563008230
Q1	TO-5	1W TA	NPN	65V	RCA	2N2102	550021020
Q2	TO5	7W TA	PNP	65V	RCA	2N4036	552040360
Q3-7	TO-92	350MW TA	NPN	25V	MOTOROLA	MPS6515	550065150
R1	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R2-4	100K	1/4W	10%		AB	TYPE CB	200101046
R5	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R6	100K	1/4W	10%		AB	TYPE CB	200101046
R7-11	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R12-13	22K	1/4W	10%		AB	TYPE CB	200102236
R14-17	100K	1/4W	10%		AB	TYPE CB	200101046
R18	1K	1/4W	10%		AB	TYPE CB	200101026
R19	3.3K	1/4W	10%		AB	TYPE CB	200103326
R20-21	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R22	100-	1/4W	10%		AB	TYPE CB	200101016
R23-24	390-	1/2W	10%		AB	TYPE EB	200203916
R25-26	10-	1/2W	10%		AB	TYPE EB	200201006
R27	1K	1/4W	10%		AB	TYPE CB	200101026
R28-29	1M	1/4W	10%		AB	TYPE CB	200101056
R30-31	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R32-33	22.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222121
R34-35	10K	1/2W			HELIPOT	66WR10K	232701034
R36	50K	1/2W	10%	200V	HELIPOT	66WR50K	232705030
R37	316K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220231631
R38	442K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220244231
R39	2K	1/2	10%		HELIPOT	66WR2K	232702023
R40	14.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214721
R41-42	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021

Table 3—6. (Cont'd).

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R43	16.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220216221
R44	316K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220231631
R45	442K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220244231
R46	14.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214721
R47	2K	1/2	10%		HELIPOT	66WR2K	232702023
R48-49	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R50	15.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215421
R51-55	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R56	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R57-58	3740-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220237411
R59	500-	1/2W	10%	200V	HELIPOT	66WR500	232705011
R60	28.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228721
R61	715-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220271501
R62	10K	1/2W			HELIPOT	66WR10K	232701034
R63	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R64-65	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R66	3010-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230111
R67	562K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220256231
R68	21.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220221521
R69	499-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249901
R70	22K	1/4W	10%		AB	TYPE CB	200102236
R71	100K	1/4W	10%		AB	TYPE CB	200101046
R72	1M	1/4W	10%		AB	TYPE CB	200101056
R73	22K	1/4W	10%		AB	TYPE CB	200102236
R74	3.9K	1/4W	10%		AB	TYPE CB	200103926
R75-78	22K	1/4W	10%		AB	TYPE CB	200102236
R79-80	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R81-82	6040-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260411
R83	500-	1/2W	10%	200V	HELIPOT	66WR500	232705011
R84	110K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211031
R85	3160-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220231611
R86	28K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228021
R87	442-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220244201
R88	5230-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220252311
R89	133K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213331
R90	2100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220221011
R91	1780-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220217811
R92	374K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220237431
R93-97	18.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220218221
R98-100	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R101	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R102	604K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260431
R103-104	6040-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260411
R106	5K	1/2W	10%	200V	HELIPOT	66WR5K	232705021
R107	4.7K	1/4W	10%		AB	TYPE CB	200104726
R110	100K	1/4W	10%		AB	TYPE CB	200101046
R111	4.7K	1/4W	10%		AB	TYPE CB	200104726
R112	1M	1/4W	10%		AB	TYPE CB	200101056
R113	22K	1/4W	10%		AB	TYPE CB	200102236
R114	10K	1/2W			HELIPOT	66WR10K	232701034
R115	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R116	715-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220271501
R118	1M	1/4W	10%		AB	TYPE CB	200101056

Table 3—6. (Cont'd).

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R119	68K	1/4W	10%		AB	TYPE CB	200106836
S49	SPDT	5A		28V	C+K	7101A	620600900
U1	8PD1L	80MW		180V	NAT.SEMI	LM1458N	500001458
U2	14 DIP-P	B/UB		CMOS	RCA	CD4066AE	510004066
U3				** NO FIXFLE **			510074260
U3	14 DIP-P			LS	T.I.	SN74LS26N	510907426
U4	14DIP-P	B/UB		CMOS	RCA	CD4025	510004025
U5	14DIP-P	B/UB		CMOS	RCA	CD4023	510004023
U6-13	8PD1L	80MW		180V	NAT.SEMI	LM1458N	500001458
U14	16DIP-P	B		CMOS	RCA	CD4060	510004060
U15	14DIP-P	B		CMOS	RCA	CD4011	510004011
U16-19	8PD1L	80MW		180V	NAT.SEMI	LM1458N	500001458
U20	14DIP-P			TTL	TI	SN7407N	510074070

Table 3—7. Dial Control/Timer C0041-13-022 A6 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C7-8	22UF	B	10%	15V	SPRAGUE	196D226X9015KA1	310802263
C9-24	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C25	.056UF		10%	100V	SPRAGUE	225P56391WD3	320005630
C26	.047UF		10%	100V	SPRAGUE	225P47391WD3	320004730
C27	091UF		10%	100V	SPRAGUE	225P91391WD3	320009130
C28	.068UF		10%	100V	SPRAGUE	225P68391WD3	320006830
C29	.056UF		10%	100V	SPRAGUE	225P56391WD3	320005630
C30-34	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C35	150PF	DB N3300	10%	1KV	CENTRALAB	DD-151	330001510
CR1-2	D035	4NS 10MA	SI	50UA	FAIRCHILD	IN4148	560041480
CR3		1W	1%	6.2V	SCHAUER	SZ6.2	562000620
Q1-2	TO-92	350MW TA	NPN	25V	MOTOROLA	MPS6515	550065150
R29-33	470K	1/4W	10%		AB	TYPE CB	200104746
R34-40	100K	1/4W	10%		AB	TYPE CB	200101046
R41	4220-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220242211
R43	3740-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220237411
R44	1.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214011
R45	4220-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220242211
R56-57	15K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215021
R58-59	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R60-61	31.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220231621
R65-66	4.7M	1/4W	10%		AB	TYPE CB	200104756
R70	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R71-75	220K	1/4W	10%		AB	TYPE CB	200102246
R76	330-	1/4W	10%		AB	TYPE CB	200103316
R77	4.7K	1/4W	10%		AB	TYPE CB	200104726
R78	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R79	4220-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220242211
R80-81	6190-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220261911
R82	3740-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220237411
R83	1.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214011
R84	4220-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220242211
U1-5	16DIP-P	B		CMOS	RCA	CD4029	510004029
U6-7	16DIP-P			TTL	TI	SN74167N	510074167
U8-9	16 DIP-P	B		CMOS	MOTOROLA	MC14585BCP	510004585

Table 3—7. (Cont'd).

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
U10-11	14 DIP-P			LS	T.I.	SN74LS90N	510907490
U12-14	16 DIP-P	B		CMOS	MOTOROLA	MC14518	510004518
U15	14DILP				MOTOROLA	K1091A-10MHZ	919200400
U16	16 DIP-P	B		CMOS	MOTOROLA	MC14516	510004516
U17-18	16DIP-P	B		CMOS	MOTOROLA	MC14015	510004015
U19	14DIP-P	B/UB		CMOS	RCA	CD4023	510004023
U20	14DIP-P	B/UB		CMOS	RCA	CD4012	510004012
U21	14DIP-P	B/UB		CMOS	RCA	CD4023	510004023
U22-23	16DIP-P	B		CMOS	RCA	CD4049	510004049
U24-28	16DIP-P	B		CMOS	RCA	CD4020	510004020
U29	16DIP-P	B		CMOS	RCA	CD4049	510004049
U33-35	16DIP-P	B		CMOS	RCA	CD4020	510004020
U36	14DIP-P	B		CMOS	RCA	CD4093	510004093
U37	16DIP-P	B		CMOS	RCA	CD4049	510004049
U38-39	14DIP-P	B		CMOS	RCA	CD4011	510004011
U40-41	16 DILP	TYPE 4	2%	100	BECKMAN	898-1-R2.2K	514500105
U42-46	8DIP-P			LM	SIGNETICS	NE 555V	510005550

Table 3—8. System I/O Board C0041-13-023 A7 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1	22UF		10%	15V	SPRAGUE	196D226X9015KA1	310802263
C2-22	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
Q1-2	TO-92	350MW TA	NPN	25V	MOTOROLA	MPS6515	550065150
R1	15K	1/4W	10%		AB	TYPE CB	200101536
R2-15	5.6K	1/4W	10%		AB	TYPE CB	200105626
R19	22K	1/4W	10%		AB	TYPE CB	200102236
R20	5.6K	1/4W	10%		AB	TYPE CB	200105626
R22-25	5.6K	1/4W	10%		AB	TYPE CB	200105626
R28-35	22K	1/4W	10%		AB	TYPE CB	200102236
R36-40	100K	1/4W	10%		AB	TYPE CB	200101046
R42-45	100K	1/4W	10%		AB	TYPE CB	200101046
U1-2	40 DIP			MOS	INTEL	8255	514001601
U3	24DIP-P			TTL	TI	SN74154N	510074154
U4-6	14DIP-P	B		CMOS	RCA	CD4013	510004013
U7	14 DIP-P			LS	T.I.	SN74LS27N	510907427
U8	14 DIP-P			LS	T.I.	SN74LS04N	510907404
U9	14 DIP-P			LS	T.I.	SN74LS04N	510907404
U10	14 DIP-P			LS	T.I.	SN74LS20N	510907420
U11	14 DIP-P			LS	T.I.	SN74LS03N	510907403
U12-13	14DIP-P	B		CMOS	RCA	CD4011	510004011
U14	14DIP-P	B		CMOS	RCA	CD4002	510004002
U15	14DIP-P	B/UB		CMOS	RCA	CD4023	510004023
U17-18	14 DIP-P	B/UB		CMOS	MOTOROLA	MC14000	510004000
U19	14DIP-P	B		CMOS	RCA	CD4001	510004001
U20	14DIP-P	B		CMOS	RCA	CD4011	510004011
U21	16DILP				RCA	CA3081	500030810
U22	14 DIP-P			LS	T.I.	SN74LS27N	510907427
U23	14 DIP-P			LS	T.I.	SN74LS20N	510907420
XU1-2	40DILP				AUGAT	540-AGID	820101400
XU3	24D1LP				AUGAT	524AGID	820101500

Table 3—9. Display I/O Board C0041-13-024 A8 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1	22UF	B	10%	15V	SPRAGUE	196D226X9015KA1	310802263
C2-14	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
Q1-15	CASE 77	40W	TC PNP	40V	MOTOROLA	MJE371	550000371
Q16-18	TO-92	350MW	TA NPN	25V	MOTOROLA	MPS6515	550065150
R1	6.8K	1/4W	10%		AB	TYPE CB	200106826
R4-19	3.3K	1/4W	10%		AB	TYPE CB	200103326
R41-54	2.7K	1/4W	10%		AB	TYPE CB	200102726
R55-68	68-	1/4W	10%		AB	TYPE CB	200106806
R69-91	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R92-106	330-	1/4W	10%		AB	TYPE CB	200103316
R107-118	220-	1/4W	10%		AB	TYPE CB	200102216
R119	1M	1/4W	10%		AB	TYPE CB	200101056
U1-2	40 DIP			MOS	INTEL	8255	514001601
U3	14 DIP-P			LS	T.I.	SN74LS27N	510907427
U5	16DIP-P	B		CMOS	RCA	CD4049	510004049
U6	14 DIP-P			LS	T.I.	SN74LS20N	510907420
U7	16DIP-P	B		CMOS	RCA	CD4029	510004029
U8	14DIP-P	B		CMOS	RCA	CD4011	510004011
U9-10	16DIP-P	B		CMOS	MOTOROLA	MC14511	510004511
U11-12	16DIP-P	B		CMOS	RCA	CD4042	510004042
U13	24DIP-P			TTL	TI	SN74159N	510074159
U14-15	16DILP				RCA	CA3081	500030810
U16-18	16DIP-P			50 V	T.I.	ULN2003AN	510075468
U19-20	16DIP-P	B		CMOS	RCA	CD4049	510004049
U22	14DIP-P			TTL	TI	SN7425N	510074250
XU1-2	40DILP				AUGAT	540-AGID	820101400
XU13	24D1LP				AUGAT	524AGID	820101500

Table 3—10. Processor B0001-01-078 A9 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-6	.01UF		00	50V	CENTRALAB	CK-103	330701030
C7	15PF DA	N330	10%	1KV	CENTRALAB	DD-150	330001500
C8	4.7UF		10%	25V	KEMET	T330A475K025AS	310004751
C9-10	.01UF		00	50V	CENTRALAB	CK-103	330701030
C11	33PF DA	N330	10%	1KV	CENTRALAB	DD-330	330003300
C12	15PF DA	N330	10%	1KV	CENTRALAB	DD-150	330001500
CR1-4	D041	1A	SI	400V	EDAL	IN4004	560040040
J2	25 DIL				BERG	65610-150	654003311
J3A	13 SIP LWR HALF				BERG	65521-113	654003123
J3B	13 SIP				BERG	65524-113	654003223
Q1	TO-92 350MW TA NPN			40V	MOTOROLA	2N3903	550039030
R1-2	3K	1/4W	5%		AB	TYPE CB	200103025
R3	4.7K	1/4W	10%		AB	TYPE CB	200104726
R4	100K	1/4W	10%		AB	TYPE CB	200101046
R5	4.7K	1/4W	10%		AB	TYPE CB	200104726
R6	1K	1/4W	10%		AB	TYPE CB	200101026
R7	3K	1/4W	5%		AB	TYPE CB	200103025
R8	1K	1/4W	10%		AB	TYPE CB	200101026
R9	1M	1/4W	10%		AB	TYPE CB	200101056
R10	10K	1/4W	10%		2	00 A410100015R71-7	200101036
R11	5.1K	1/4W	5%		AB	TYPE CB	200105125
R12	390-	1/4W	10%		AB	TYPE CB	200103916
R13	3K	1/4W	5%		AB	TYPE CB	200103025
R14	5.1K	1/4W	5%		AB	TYPE CB	200105125
R15	270-	1/4W	10%		AB	TYPE CB	200102716
R16	1K	1/4W	10%		AB	TYPE CB	200101026
R17	390-	1/4W	10%		AB	TYPE CB	200103916
R18-19	4.7K	1/4W	10%		AB	TYPE CB	200104726
S1	SPDT				CONTROL SW	B8600	635201401
U1-2	14 DIP-P		LS		TI	SN74LS15N	510907415
U3	14DIP-P		TTL		TI	SN7400N	510074000
U4-6	16DIP-P		TTL		TI	SN74367N	510074367
U7	SYSTEM CONTROLLER				INTEL	8228	514001402
U8	CLOCK GENERATOR				INTEL	8224	514001401
U9	MICRO-PROCESSOR,8 BIT				INTEL	8080A	514001400
U10	16DIP-P	B	CMOS		RCA	CD4060	510004060
U11	ASYNC.COMM.INTERFACE ADAP				MOTOROLA	MC6850L	514003501
XU7	28 DIP				AUGAT	528-AG10D	820101501
XU8	16DIP				AUGAT	516-AG10D	820101703
XU9	40DILP				AUGAT	540-AGID	820101400
XU11	24D1LP				AUGAT	524AGID	820101500
Y1	CRYSTAL 18 MHZ				INTERNAT'L	HC-18	919100010
Y2	PAR RES. 500 OHMS				INTERNAT'L	HC-18, 3.6045MHZ	919100003

Table 3—11. Memory Board B0041-13-041 A10 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
U8	U8 PROM IDENTIFIER						A004113075
U9	U9 PROM IDENTIFIER						A004113074
U11	U11 PROM IDENTIFIER						A004113077
U12	U12 PROM IDENTIFIER						A004113076
U1, 5	14DIP-P		TTL		TI	SN7432N	510074320
U2	14DIP-P		TTL		TI	SN7400N	510074000
U3, 6	16DIP-P	125MW	TTL		TI	SN74155N	510074155
U4, 7	16DIP-P		TTL		TI	SN74367N	510074367
U15-22	RAM,1KX1				INTEL	2102A	514000401
C1, 3, 6	10UF	B	20%	20V	SPRAGUE	196D106X0020JA1	310801060
C2, 4-5, 7-16	.01UF		00	50V	CENTRALAB	CK-103	330701030
J2	25DIL				BERG	65610-150	654003311

Table 3—12. TTY Interface B0041-13-064 A11 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-4	22UF		B 10%	15V	SPRAGUE	196D226X9015KA1	310802263
C5-6	.22UF	MD Y5V	20%	50V	ERIE	8131-050-651-224M	330802240
C7-27	.01UF		00	50V	CENTRALAB	CK-103	330701030
CR1-4	D041	1A	SI	800V	EDAL	1N4006	560040060
CR5	A1	200NS 1A	SI	.1MA	MOTOROLA	1N4934	560049340
CR6	A31A	1W	5%	24V	DICKSON	1N30293	562030292
F1		.1A		250V	LITTELFUSE	3AG	863100100
J35	10 DIL				BERG	65610-120	654003326
R1-2	500-	3W	5%		W LEONARD	TYPE 3X	210305015
R3	1M	1/4W	10%		AB	TYPE CB	200101056
R4-5	3.3K	1/4W	10%		AB	TYPE CB	200103326
R6	470-	1W	10%		AB	TYPE GB	200304716
R7-8	560-	1/2W	10%		AB	TYPE EB	200205616
R10-11	500-	3W	5%		W LEONARD	TYPE 3X	210305015
R12	180-	1/4W	10%		AB	TYPE CB	200101816
S1	DIP SWITCH,8 POSITION				CTS	206-008	640001000
S2	DIP SWITCH 5 POSITIONS				SAE	1005-692	640001001
U1-2	28DIL				INTEL	8251	514001602
U3	18 DIL				WEST.DIGIT	BR1941L	514001700
U4	6 DIP-P				MOTOROLA	MOC8050	515000103
U5	TTY-U5 PROM						A004113078
U6	TTY U6 PROM						A004113079
U7	16 DIP-P			DS	T.I.	SN75152N	510075152
U8	8DIP-P			DS	TI	SN75150P	510075150
U9	14DIP-P			TTL	TI	SN74132	510074132
U10	16 DIP-P			LS	TI	SN74LS138N	510974138
U11	16 DIP-P			LS	T.I.	SN74LS139N	510974139
U12	16 DILP	TYPE 4	2%	100	BECKMAN	898-1-R2.2K	514500105
U13	14 DIP-P			LS	T.I.	SN74LS20N	510907420
U14-15	14DIP-P			TTL	TI	SN74125N	510074125
U16	14 DIP-P			LS	T.I.	SN74LS32N	510907432
XF1-2	FUSECLIP,PC MTG,FUSE STOP				LITTLEFUSE	102068	863300301
XU1-2	28 DIP				AUGAT	528-AG10D	820101501
XU5-6	24PIN				BURNDY	DILB-24P-108	820101502
Y1	CRYSTAL 5.0688 MHZ				INTERNAT'L	HC-18	919100009

Table 3—13. Card Cage Assembly D0041-13-047 A12 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
A1	MOTHER BOARD 96831						D004113011
A2	SLEEVE HOLDING CKT MOD						B004113033
LS1	SPEAKER 45 OHM				QUAM	25A07-Z45	926000200

Table 3—14. Mother Board D0041-13-011 A12A1 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
CABLE	CABLE-#39						A004113039
CR1-3	D035 4NS 10MA	SI	50UA		FAIRCHILD	IN4148	560041480
J1-3	50PIN				3M CO.	3433-2003	654000400
J4	16 DIP				BURNDY	DILB16P-108	820101100
J5	20 PIN				3M	3428-1002	654000500
J6	16 DIP				BURNDY	DILB16P-108	820101100
J8	50PIN				3M	3433-1002	654000401
J9-10	16 DIP				BURNDY	DILB16P-108	820101100
J11	16 COND				AMP	350214-1	650900900
Q1	TO-3 20W(MAX)		5%	-5V	NAT SEMI	LM320KC	500003200
XA1-2	22 POS				CDC	VPBJ4E22E00A1	651800108
XA3-8	50 POS				SAE	CPH8100-100	651800007
XA9-12	22 POS				CDC	VPBJ4E22E00A1	651800008

Table 3—15. Sleeve Holding Circuit B0041-13-033 A12A2 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
Q1	MODTO220	40W TC	PNP	100V	TI	TIP32C	552000323
CR1-2	D041	1A SI		800V	EDAL	IN4006	560040060
CR3	TRANZORB, BV	58.9 to 65.1			GEN SEMI	1.5KE62A	565500002
CR4	A140	1W	1%	9.1V	SCHAUER	SZ9.1	562000910
R1	47—	3W	5%		OHMITE	4379	210304705
R2	330—	½W	10%		AB	TYPE EB	200203316
R3	120—	½W	10%		AB	TYPE EB	200201216

Table 3—16. Front Panel Assembly D0041-13-045 A13 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
M1	METER,41-3A,500-0-500 UA				MODUTEC	750-099	900000004
R1-5	PANEL POT MODIFICATION						A004113205
R6	50K-50K AUDIO T 20%				CRL	BAS1209	238005030
S40	2C-2C CONTACT				S CARLSON	173N	630100600
S41-42	DPDT	5A		28V	C+K COMP	7211P3YZB	620401000
A1	PC ASSY 96821 PRGM I						B004113013
A2	PC ASSY 96820 PRGM II						B004113012
A3	PC ASSY 96813 DISPLAY BD						D004113010
A4	PC ASSY 96829 KEYBOARD						B004113017
A5	LO LEVEL SWITCH ASSY						B004113029
A6	EML SWITCH ASSY						B004113030
A7	HI LEVEL SWITCH ASSY						B004113031
A8	LINE CONTROL MODULE ASSY						D004113048
P39	4 COND				AMP	1-480426-0	650900101
P39	PIN MATE-N-LOCK LOOSE				AMP	60618-1	863400430
S1	DPDT	5A		28V	C+K COMP	7201P3YZB	620400600

Table 3—17. Programmer I B0041-13-013 A13A1 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
CR1-4	D035 4NS 10MA SI 50UA				FAIRCHILD	IN4148	560041480
J4	16 DIP				BURNDY	DILB16P-108	820101100
S9-12	2C				CRL	2KAB010000XXX	635800700
S9-12	1/8				CRL	J64286	858700180

Table 3—18. Programmer II B0041-13-012 A13A2 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
CR1-8	D035 4NS 10MA SI 50UA				FAIRCHILD	IN4148	560041480
J6	16 DIP				BURNDY	DILB16P-108	820101100
S16-23	2C				CRL	2KAB010000XXX	635800700
S16-23	1/8				CRL	J64286	858700180

Table 3—19. Display Board D0041-13-010 A13A3 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
CR17-32	D035 4NS 10MA SI 50UA				FAIRCHILD	IN4148	560041480
CR33-90	L.E.D.,RECTANGULAR,RED				H.P.	5082-4670	564501100
CR91-102	10 MA				H.P.	HLMP-1301	564500805
CR103-112	L.E.D.,RECTANGULAR,RED				H.P.	5082-4670	564501100
J1-2	50PIN				3M CO.	3433-2003	654000400
R1-5	22-	1/4W	10%		AB	TYPE CB	200102206
R6	130-	1/4W	5%		A.B.	TYPE CB	200101315
R7-27	22-	1/4W	10%		AB	TYPE CB	200102206
R28	130-	1/4W	5%		A.B.	TYPE CB	200101315
R29	22-	1/4W	10%		AB	TYPE CB	200102206
R30	130-	1/4W	5%		A.B.	TYPE CB	200101315
R31-33	22-	1/4W	10%		AB	TYPE CB	200102206
R34-37	130-	1/4W	5%		A.B.	TYPE CB	200101315
R46	130-	1/4W	5%		A.B.	TYPE CB	200101315
S24-39	SPDT	1A		28V	C&K	8121	635200700
U1-17	14PDIL	20MA RED			HP	5082-7650	728301701

Table 3—20. Keyboard B0041-13-017 A13A4 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
CR1-18	D035 4NS 10MA		SI	5CUA	FAIRCHILD	IN4148	560041480
J3	50PIN				3M CO.	3433-2003	654003400
S44	BLACK	GLOSS			DIGITRAN	29119G/P-7	626801300
S45	KEYBOARD	SWITCH,1A CONT.			CLARE	S82010	635000400
S45		GREY			CLARE	KA-1702-LZ	976000600
S45		GREY			CLARE	KA-0009-LZ	976000601
S45		GREY			CLARE	KA-0028-LZ	976000602
S45		GREY			CLARE	KA-0029-LZ	976000603
S45		GREY			CLARE	KA-0030-LZ	976000604
S45		GREY			CLARE	KA-0031-LZ	976000605
S45		GREY			CLARE	KA-0032-LZ	976000606
S45		GREY			CLARE	KA-0033-LZ	976000607
S45		GREY			CLARE	KA-0034-LZ	976000608
S45		GREY			CLARE	KA-0035-LZ	976000609
S45		GREY			CLARE	KA------LZ	976000610
S45		GREY			CLARE	KA------LZ	976000611

Table 3—21. Low Level Switch Assembly B0041-13-029 A13A5 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R1	15K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215021
R2	187K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220218731
R3	11K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211021
R4	69.8K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220269821
R5	7.32K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220273211
R6	169K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220216931
R7	6190-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220261911
R8	44.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220244221
R9	4320-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220243211
R10	3740-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220237411
R11	60.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260421
R12	3090-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230911
R13	51.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251121
R14	2550-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220225511
R15	59K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220259021
R16	2100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220221011
R17	137K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213731
R18	1780-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220217811
R19	174K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220217431
S13		1A		28V	OAK	269430-F2	625801200

Table 3—22. EML Switch Assembly B0041-13-030 A13A6 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R1	590-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220259001
R2	9090-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220290911
R3	750-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220275001
R4	17.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220217421
R5	976-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220297601
R6	25.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220225521
R7	1.24K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212411
R8	1780-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220217811
R9	28K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228021
R10	2370-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223711
R11	88.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220288721
R12	3400-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234011
R13	113K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211331
R14	5230-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220252311
R15	121K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212131
R16	9090-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220290911
R17	137K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213731
R18	22.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220222121
R19	150K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215031
S14		1A		28V	OAK	269430-F2	625801200

Table 3—23. High Level Switch Assembly B0041-13-031 A13A7 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R1	232K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223231
R2	42.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220242221
R3	178K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220217831
R4	17.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220217421
R5	11.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211321
R6	8.06K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220280611
R7	7870-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220278711
R8	27.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227421
R9	5.62K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220256211
R10	33.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220233221
R11	5.62K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220256211
R12	12.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212421
R13	4220-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220242211
R14	13K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213021
R15	4220-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220242211
R16	7150-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220271511
S15		1A		28V	OAK	269430-F2	625801200

Table 3—24. Line Control Module Assembly D0041-13-048 A13A8 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C7	2.16UF		2%	400V	N.TELECOM	CM01Y-2.16UFG400	335321640
S8	SWITCH ASSEMBLY S8						A004113059
J12-13, 16-17	SPECIAL				SWCRFT	5J-1564	650402100
J14-15	CKT 20				TEC. COMP	353C5N	650400004
A1	PC ASSY LINE CONT.						A004113014
A2	LOOP/LEAK SWITCH ASSY						A004113053

Table 3—25. Line Control Board B0041-13-014 A13A8A1 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-5	1.0UF ME		Y5V	20% 100V	ERIE	8141-100-651-105M	330801051
C6	20UF			50V	SPRAGUE	TE1305	300202061
J8	50PIN				3M CO.	3433-2003	654000400
L1	TALK COIL				CECO	CE-104A	450100100
R1-2	900-	5W	5%		W LEONARD	TYPE 5XM	210409015
R3	100K	1/2W	5%		AB	TYPE EB	200201045
R4	1K	1/2W	10%		AB	TYPE EB	200201026
S2-3	4C				CRL	2KAB001000XXX	635800800
S2-7	3/32				CRL	J64284	858703320
S4-5	2C				CRL	2KAB010000XXX	635800700
S6-7	4C				CRL	2KAB001000XXX	635800800

Table 3—26. Loop/Leak Switch Assembly B0041-13-053 A13A8A2 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R1	600-	1/2W	1%		ELECTRA	RN65 SIZE 100 PPM	220660001
R2-3	200-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220001
R4-9	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R10	200-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220001
R11	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R12	600-	1/2W	1%		ELECTRA	RN65 SIZE 100 PPM	220660001
R13-14	10.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210221
R15	4420-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220244211
R16	7150-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220271511
R17	348-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234801
R18	2.49K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220224911
R19	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
S43	1DICK12P 2DICK9P0				CRL	A77-461	624900102

Table 3—27. Rear Panel Assembly D0041-13-046 A14 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
F1-2		2A		250V	BUSSMAN	MDL	863101700
J34	3-PIN	6A		250V	BELDEN	17252	652201700
P39	4 COND				AMP	1-480426-0	650900101
P39	PIN MATE-N-LOCK LOOSE				AMP	60618-1	863400400
PSU1	PWR SUPPLY,5V6A,+12-12,1A				DELTRON	QT2-C3	960104004
PSU2		1.5A		12V	DELTRON	8927X	960104003
S48	SWITCH ASSEMBLY S48						A004113058
XF1-2	FUSEHOLDER,3AG PANEL				BUSSMAN	HKP	863000100
B1	FAN MUFFIN				ROTRON	M747 VENTURI	920000100
S46	INTERLOCK SWITCH W/CHEAT				MICROSWITCH	2DM409	600000001
A1	PC ASSY INC. CKT						A004113015
A2	MCS MODULE						A004113049

Table 3—28. Incoming Circuit B0041-13-015 A14A1 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1	4UF		10%	150V	F-DYNE	MPE11-4.0-150-10	321904050
C2-3	1UF		10%	150V	F-DYNE	MPE12-1.0-150-10	321901051
C4	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C5-6	.01UF		1%	100V	F-DYNE	PS11-01-100-1	321501031
C7	.01UF		10%	100V	SPRAGUE	225P10391WD3	320001030
CR1-4	D035	4NS 10MA	SI	50UA	FAIRCHILD	IN4148	560041480
CR11	D041	1A	SI	800V	EDAL	1N4006	560040060
CR12-15	D035	4NS 10MA	SI	50UA	FAIRCHILD	IN4148	560041480
J9	16 DIP				BURNDY	DIL816P-108	820101100
K1	RELAY,REED,PC2AMUSTOP			4V	MIDTEX	172-124BA1	604103100
Q1-2	TO-92	350MW TA	NPN	25V	MOTOROLA	MPS6515	550065150
Q3	TO92	350MW TC	PNP	25V	MOTOROLA	MPS6519	552065190
Q3			** NO FIXFLE **				552068190
Q4	TO-92	350MW TA	NPN	25V	MOTOROLA	MPS6515	550065150
R1-2	100K	1/2W	10%		AB	TYPE EB	200201046
R3	47K	1/2W	10%		AB	TYPE EB	200204736
R4-5	4.7K	1/4W	10%		AB	TYPE CB	200104726
R6	1M	1/4W	10%		AB	TYPE CB	200101056
R7	8.2K	1/4W	10%		AB	TYPE CB	200108226
R7			** NO FIXFLE **				200158226
R8-9	100-	1/2W	10%		AB	TYPE EB	200201016
R10	5.6K	1/4W	10%		AB	TYPE CB	200105626
R11	499-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249901
R12	900#	3W	5%		W LEONARD	TYPE 3X	210309015
R13	8660-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220286611
R14	78.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220278721
R15	10K	.75W	10%		HELIPOT	89PR10K	232501030
R16	100-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210001
R17	13K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213021
R18	15K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215021
R19	5K	.75W	10		HELIPOT	89PR5K	232505020
R20	100K	1/2W	10%		AB	TYPE EB	200201046
R21	470K	1/2W	10%		AB	TYPE EB	200204746
R22	100K	1/2W	10%		AB	TYPE EB	200201046
R23	47K	1/2W	10%		AB	TYPE EB	200204736
R24	22K	1/4W	10%		AB	TYPE CB	200102236
R25	1M	1/4W	10%		AB	TYPE CB	200101056
R36	86.6-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220286691
RT1	8K				FENWALL	GB38V2	290108020
T1	XFMR,P40/50SPL,400/500CT				UTC	PCS0-13	400300600
TB1	5 TERM				MAGNUM EL.	2022-05-06	850101900
U1	14DIP-P	8		CMOS	RCA	CD4001	510004001
U2-3	16DIP-P	8		CMOS	RCA	CD4020	510004020
U4	14DIP-P	8		CMOS	RCA	CD4013	510004013
U5	14DIP-P	8		CMOS	RCA	CD4093	510004093
U6	8PD1L	80MW		18V	NAT.SEMI	LM1458N	500001458

Table 3—29. MCS Module D0041-13-049 A14A2 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
J18-33	SPECIAL				SWCRFT	5J-1334	650401400
CR1-6	D041	1A	SI	800V	EDAL	1N4006	560040060
J10	16DIP				ROB NUGENT	ICL-163-56-G	820101100
K1-8	130—			12V	NIPPON	MR11N53	600601300
K9	1A PC			12V	MIDTEX	172-111C00	604106400

SECTION 4

PERFORMANCE SPECIFICATIONS

4.1 This section gives performance specifications for the TTS 41-3A printed circuit assemblies. These specifications are given in numerical order; with each document number corresponding to the Northeast Electronics part numbers shown in Sections 2 and 3.

4.2 Printed circuit cards A9 and A10 comprise a standard Intel MCS-80 microprocessor chip set. The devices employed in this microprocessor are fully described in the MCS-80 User's Manual and in related documentation available from Intel. Intel publications can also be referred to for detailed information on other 8000 series integrated circuits found on cards A7, A8, and A11.

PERFORMANCE SPECIFICATION FOR
BASIC MICROPROCESSOR SYSTEM CARD

1. SCOPE

This document describes the testing of the Basic Microprocessor System Card (BMSC). The Basic Microprocessor System Card is not a unit for sale by itself, rather it is intended for inclusion within other Northeast products. As such, it is manufactured as a standard assembly. This assembly may be used as is (with appropriate ROM (Read Only Memory) for the particular set) or may be modified as specified by the particular project engineer for inclusion within his test set. This procedure describes the minimum configuration card. The basic system requirement is that the system execute all instructions correctly in any order.

It is assumed that the user of this specification will have on hand the various references. They are necessary to understanding this specification. It is the responsibility of Test Engineering to determine the exact diagnostics used. This document defines the generic type of testing required.

2. APPLICABLE DRAWINGS: LIST ASSY#, SCHEMATIC #, ETC.

The BMSC (Basic Microprocessor Sysrem Card)configuration consists of two 4¼ x 6 cards operating together. These cards are described in the following drawing.

1. 0001-00078 --- Proc. Card
2. 0001-00079 --- Memory Card
3. 378 --- Schem. List
   379 --- Schem. List
   478 --- This Specification

Each of these cards run from the same voltages. These voltages should be 12 plus

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	ENGR.	DATE
BASIC MICROPROCESSOR SYSTEM CARD PERFORMANCE SPEC.	DRAWING NO. A-0001-00478	REV

NEC-100R-0776

or minus 5%, 5 plus or minus 5% and minus 5 Volts plus or minus 5%.

Also included in the card is a power-up delay circuit consisting of a RC combination feeding the Intel 8224 clock chip. In parallel with the capacitor is the reset push-button. (.1 to .4 secs) During normal operation when power comes up, enough delay is present to insure proper initial operation of the processor. A sufficient test of this circuit is that when power is applied the card should come up running.

An additional fact of the power-up sequence is the power-up flip-flop. Initially the ROM (Read Only Memory) at 8000 is forced to occupy 000-3FF as well as 8000-83FF. The first operation of a program is to jump to 8003. The first write to memory resets the F-F returning the card address lines to norm.mode (RAM,Random Access Memory 0-3FF, ROM, Read Only Memory 8000-83FF). This allows the system designer to reconfigure the "resets" to his best advantage. Except for power-up this F-F will normally be of no concern.

A crystal is on the card which interconnects to the 8224 forming an oscillator. With the crystal used the clocks applied to the 8080A will be 2.025MHZ plus or minus 0.1%. This may easily be checked with the aid of an oscilloscope. Also on the card is a TTY Drive Circuit. This is designed to interface with Teletype Corp., Model 33 machine. (See schematic).

The connections between the two cards may be made via a 50 pin ribbon cable or via the 44 pin PC edge connector. The interconnections are on a one for one basis. For more details see the referenced engineering documents.

The major elements of this processor card are:

A. Intel or equivalent 8080A microprocessor

B. 8214 clock generator chip

C. 8228 system controller

D. 2101A Random Access Memory

E. 6850 asyncronous interface element

Each of these elements performs its particular task within the processing job. Due to the high level operation of each component, it is not felt practical to provide the usual blow by blow description. A fairly lucid description is given in the 8080 System Designer's Manual, published by Intel Corp. This work should be consulted for details of the processor system.

3. In general, the operation of a microprocessor is orchestrated by a central clock. Once having examined the clock for proper operation, an appropriate diagnostic ROM (Read Only Memory) is inserted into the processor. In the event that the processor functions more or less correctly, debug may begin. Although the exact details of the tests will be determined by the Test Department, certain general tests are to be performed.
The minimum operational configuration is 1-2708 type ROM (Read Only Memory), the 8080 processor, and the Motorola 6850 ACIA. For this reason it is STRONGLY recommended that every effort be taken to obtain a high yield from the assembly process. In particular the use of pretested IC's and pretested boards is recommended.

4. PRACTICAL TESTS

The following tests are felt to be minimal:

1. Using an oscilloscope, verify that the proper clock waveforms are present on the CPU (Central Processor Unit). (Ref. 1,Page 2-8).
2. Insert a test program to wiggle all the address lines, verify that each wiggles at the proper rate and that none are shorted to each other.
3. Verify that the diagnostic ROM (Read Only Memory) has the correct check sum. This assures that all the data and addresses are more or less correct.
4. Run marching ones, marching zeros, as a RAM (Random Access Memory) diagnostic. Each minute this routine will print a symbol to indicate proper operation.
5. Run an ACIA Mot. 6850 diagnostic to verify proper operation of TTY interface (which must be more or less correct for the initial diagnostics to run).
6. The PIA (Mot. 6820) is not available with the "vanilla flavored" card. Engineers specifying the use of this chip are responsible for specifying its tests.
7. Assuming proper operation thus far an overall diagnostic should be run to test the system for the presence of any partial shorts which might cause erratic operation. This diagnostic should be a combination of RAM, ROM, ACIA, and CPU usage designed to execute typical types of programs. It should run for a minimum of one minute and print a message to indicate each time the whole program is successfully passed.

5) OTHER INFORMATION

The operation of a processor requires a level of performance one step above that usually required from analog and digital compoents. In addition to all the timing requirements being met, all the various voltage levels must be correct. It is not practical to specify each voltage and timing relationship which must be maintained to insure proper operation. It is expected that a properly trained technician will be available to guide the testing of faulty boards. To reiterate it IS imperative that every step be taken to insure that the maximum practical yield from assembly process.

REFERENCES:

8080 System Designers Handbook - Intel Corp.

6500 Hardware Manual - MOS Technology, Inc.

Engineering Memo: Power Requirements of BMSC
Oct. 23, 1975 J. Harrison & R. Rock

Super Card Connection
3/8/76 RWR

Motorola M6800 Systems Reference and Data Sheets

ENGINEERING NOTES ON THE BMSC PERFORMANCE SPECIFICATION

The following notes are intended to provide helpful hints on the tests mentioned in the BMSC Test Specification.

1. When testing the Clock and Address, one of the most powerful and useful techniques is to check for the proper appearance of the voltage levels. During normal operation of an MPU the voltage will either be a logic one or a zero. This gives a picture on the scope which appears on a slow sweep to have two distinct levels. When lines are shorted to each other appear to be three levels(or more) by simply running the scope probe (of a scope fast enough to follow the signals across the address lines) one can quickly spot lines which are different. Frequently two adjacent lines will appear to be the same. Combined with the three level observations this virtually proves a case of shorted lines.

2. Another useful trick is to sync. the scope on the PIA select pulse. This pulse in most programs will only occur each program loop. Thus the waveforms observed throughout the card will appear stationary. One again probes the various circuit points for strange appearing levels and/or rinse times. With the stationary picture a judicious finger may be paralleled with the scope probe. The portions of the bus or line which are floating as a result of the tri-state operation will wiggle as a result of the induced 60 HZ.

3. When examining the address lines, the highest lines will be usually seem to have a net wiggle of the slowest frequency. The actual observed rates will depend on the program but again experience will quickly lead one to unusual lines.

4. The first step in the diagnostic test of the BMSC system is to check the sum of all the bytes in the ROM. This test assures that the system is basically sound and in particular that the PROM program has not changed as a result of leaky bits in the PROM.

5. Marching ones and marching zeros tests the system RAM to insure that no major problems are present. The testing of RAM is an art unto itself. This minimal test verifies that RAM is basically OK. One should not rule out the possible existance of pattern sensitivities based upon successful completion of this test.

6. Run an ACIA diagnostic to verify proper interrupt operation as well as correct operation of the ports of the aCIA. (The ACIA must be basically OK for the prior tests to run).

NORTHEAST ELECTRONICS int CONCORD, NH, U S A	DRAWN BY	SCALE
	ENGR.	DATE
BASIC MICROPROCESSOR SYSTEM CARD PERFORMANCE SPEC.	DRAWING NO. A0001-00-478	REV

NEC-1000R-0776

7. BNR MAZE program is a test program to verify that each instruction in the 8080 is executed correctly. It is successfully executed when it returns from your call to it. In the event of failure, the CPU is most probably a defective component.

8. The last test is intended to insure that a minimum level of system reliability exists. A potpouri of diagnostics including those above should be run for a minimum of 10 minutes to verify that no marginal conditions are present.

Due to the complexity of the BMSC, one will occasionally encounter bugs which are very difficult to find. With the "raw" yield from assembly at about 95% of these should be set aside for further study. In the few cases where these units are not fixable, the pluggable parts should be removed and re-routed for incoming quality assurance and then back into stock for reuse. The defective boards should be discarded.

A strap selectable wait-state is available for use with slow memories (access > 500 nsec) by connecting the 'WT' and 'RDY' test points together. This configuration causes a single Ø2 period wait after addressing, and before reading or writing.

41-3A DISPLAY BOARD

A-0041-13-410

I. APPLICABLE DRAWINGS:

D-0041-13-010
D-0041-13-310
9700-96813

II. SCOPE:

This document covers the pertinent operating and test procedures for the 41-3A display board. The board may be tested either manually, or by semi-automatic fixture.

III. GENERAL:

This display board consists of two groups of multiplexed 7-Segment displays, several continuous running LED's, and two switch groups. All LED's are high efficiency, and should be run at no more than 20 mA continuous current per segment. The switches are normally open, operating in two groups. The switches are diode blocked from each other, with each group having an enable lead common.

Testing may be done in three sections:

7-Segment displays
individual leds
switch groups

7-Segment Testing

The 7-Segment displays are operated in two groups, the two line displays (U1 & U2) having common segments tied together.

Segment	I/O Line
A	J2.18
B	J2.20
C	J2.26
D	J2.28
E	J2.30
F	J2.22
G	J2.24

These lines are taken low to activate the segments, while the enable line for the display chip is taken to +5 volts.

NORTHEAST ELECTRONICS Int CONCORD, NH, U.S.A.		DRAWN BY	SCALE
		ENGR.	DATE
41-3A DISPLAY BOARD		DRAWING NO. A-0041-13-410	REV

NEC-100R-0776

U1 is enabled when J2.13 is taken to +5 volts.

U2 is enabled when J2.42 is taken to +5 volts.

The second group of 7-Segment displays consists of the Dial Number, and Accumulator sections. Both sections have all individual segments tied together on a bus. Segments are selected by applying a ground to the lines per the following table:

Segment	I/O Line
A	J1.42
B	J1.43
C	J1.45
D	J1.44
E	J1.40
F	J1.41
G	J1.46

The digits are selected by taking the enable lines to +5 volts, per the table below:

Digit	I/O Line
U3	J2.13
U4	J2.15
U5	J2.17
U6	J2.23
U7	J2.25
U8	J2.27
U9	J2.50
U10	J2.48
U11	J2.42
U12	J2.44
U13	J2.46
U14	J1.13
U15	J1.15
U16	J1.19
U17	J1.21

Enabling one display should not enable another, except in the case of U1-U3, and U2-U11 combinations. The same applies on a segment basis;

No two different segments should turn on when one segment line is enabled.

Individual Led Testing

Most of the individual leds are current limited, and the enable lines need only be taken to ground, with +5 volts applied to:

J1.16
J1.18
J2.32
J1.12
J1.14

The enable lines will be called out by the display panel designations, rather than diode numbers.

Panel Indicator	Enable Line	
inter. dig. pd.	J2.11	
idle	J2.7	
on hook	J2.1	
tty	J2.5	
wsd	J2.9	
dialing	J2.37	
wtr	J2.41	
test ok	J2.43	
uta	J2.14	
utb	J2.4	
idle a	J2.12	
idle b	J2.8	
trace a	J2.10	
trace b	J2.6	
busy a	J2.16	
busy b	J2.2	
system held	J2.39	
over range	J2.45	
pwr int	J2.47	
prog error	J2.49	
no dialtone	J1.10	Require external 220 ohm current limiting resistor
open c-lead	J1.8	
rev drng dial	J1.6	
reorder	J1.4	
reo + ans	J1.7	
busy + ans	J1.17	
busy	J1.31	
lo level	J1.37	
no khz	J1.47	
hi level	J1.49	
no answer	J1.48	
inc ckt flt	J1.50	

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DRAWN BY		SCALE
ENGR.		DATE
41-3A DISPLAY BOARD	DRAWING NO. A-0041-13-410	REV

NEC-100R-0776

Switch Testing

The switches are arranged in two groups, each group having a select line. This line is normally high, and is taken low when the group is to be read. The switches are diode blocked from each other, and operate on a switch data bus. Switches are normally open, closing when pushed, momentary.

A 'high' is normally +5 volts, a low is ground.

switch	select line	data bus pin
reo+ans	J1.9	J1.36
bsy+ans		J1.30
busy		J1.28
lo level		J1.26
no khz		J1.34
hi level		J1.32
no ans		J1.24
inc ckt		J1.22
reset	J1.2	J1.36
ok test		J1.30
a channel		J1.28
b channel		J1.26
no dial tone		J1.34
open c-lead		J1.32
rev drng dial		J1.24
reorder		J1.22

This board is the input/output device for the operator, so it is relatively important that the leds used for backlighting be neatly arranged. This neatness is important since the leds do not have a wide dispersion angle.

The leds, and diodes should not be subjected to more than 20 mA forward, current, and 6 volts reverse bias should not be exceeded.

NORTHEAST ELECTRONICS int CONCORD, NH, U.S.A.		DRAWN BY	SCALE
		ENGR.	DATE
NEC-100R-0776	41-3A DISPLAY BOARD	DRAWING NO. A-0041-13-410	REV

MOTHERBOARD

A-0041-13-411

I. APPLICABLE DRAWINGS:

D-0041-13-011 Assembly
E-0041-13-311 Schematic
9700-96831 Hole Schedule

II. SCOPE:

This document covers the test requirements for the motherboard only, not any of the cardcage assembly.

III. GENERAL:

This performance specification covers the special data required to test this motherboard. The listed schematic should be used to check out continuity between all card edge connectors, sockets, and quick disconnect pins. The AC cable may be tested separately, or at this level. The only requirement on the AC cable (cable 39) is that pin one at each end be connected to pin one at the other, etc., a 1:1 correspondence.

The only portion of the motherboard that may be difficult to check is the active components, the 3 diodes, and the voltage regulator. The diodes should not be reverse biased by more than 20 volts, nor forward current exceed 10 mA. The diodes must not exhibit abnormal leakage for silicon.

The -5 volt regulator will be more difficult to test, and may affect the lines to which it is attached; ground, -12, and -5 volts for XA9-XA12. Voltage polarity from ground to -12 must not be reversed, and power should not be applied to the -5 volt line of XA9-XA12, or damage to the regulator may result. For this reason, if the motherboard is placed on the ADDISON, all pins attached to the regulator or diodes should not be tested.

NORTHEAST ELECTRONICS itt CONCORD, NH, U.S.A.		DRAWN BY	SCALE
		ENGR.	DATE
MOTHERBOARD		DRAWING NO. A-0041-13-411	REV

NEC-100R-0776

PROGRAMMER II

A-0041-13-412

I. APPLICABLE DRAWINGS:

B-0041-13-012	Assembly
B-0041-13-312	Schematic
9700-96820	

II. SCOPE

This document covers the pertinent design and test requirements for the PC board only.

III. GENERAL:

The switches on this board are divided into two groups each having its own access line. The operation and access of one group should have no effect on the other group. The select line is normally held at +5 Volts and taken to ground when the group is accessed. The diodes in the circuit are used to block closures of one switch affecting the lines associated with another switch. Only one group is accessed at a time.

When testing the board do not exceed 20 volts reverse bias on the diodes. Do not exceed 10mA forward current through the diodes. At this forward current the voltage drop of a diode should not exceed 1 Volt. The normal operating current of a diode is .5mA.

NORTHEAST ELECTRONICS itt CONCORD, NH, U.S.A.		DRAWN BY	SCALE
		ENGR.	DATE
PROGRAMMER II		DRAWING NO. A-0041-13-412	REV

NEC-100R-0776

PROGRAMMER I

A0041-13-413

I. APPLICABLE DRAWINGS:

B-0041-13-013	Assembly
B-0041-13-313	Schematic
9700-96821	Hole Schedule

II. SCOPE:

This document covers the pertinent design and test requirements for the PC board only.

III. GENERAL:

The PC Board serves as both a switch mounting and interconnect board. The interconnect portion consists of ten quick disconnect lugs electrically tied to ten pins on the flat cable socket.

The switches have one common line that in normal operation is taken from + 5 Volts to Gnd when the switch group is accessed. The diodes are used to block the closure of one switch from affecting any other switch lines. When testing be sure that the diodes are good and in the right direction as a shorted diode will cause havoc with the rest of the system.

When testing the reverse voltage applied to the diodes should not exceed 20 Volts and the forward current should be limited to 10mA. When a diode is conducting in the forward direction its voltage drop should not exceed 1 Volt at 10mA. The normal operating current of the diode will be .5mA.

NORTHEAST ELECTRONICS nt CONCORD, NH, U.S.A.		DRAWN BY	SCALE
		ENGR.	DATE
PROGRAMMER I		DRAWING NO. 0041-13-413	REV

NEC-100R-0776

I. INCOMING CIRCUIT

Applicable Drawings:

B0041-13-015	Assembly
D0041-13-315	Schematic
9700-96826	

Scope:

This document contains circuit description, test specifications, and applicable test techniques to check the incoming circuit board.

General:

The incoming circuit is essentially composed of a ringing detector, a stable 1004 Hz milliwatt, and a sleeve sensor. Only two adjustments are available for frequency and level adjustment of the milliwatt.

II. CIRCUIT DESCRIPTIONS AND TESTS

Ringing Detector:

This ringing detector is a non-adjustable circuit design to trip during the first ring cycle--meeting the following requirements:

a) Frequency of ringer greater than 16 Hz.

b) Ring duration greater than 600 milliseconds.

c) Tip to gnd, Ring to gnd, Ring to Tip — Voltage greater than 65 Vrms

C1 and R3 form a pre-trip ringer impedance of approximately 49K Ohms. The ringing signal is DC blocked by C2 and C3. This signal, if present will cause $U1_a$ or $U1_b$ to switch from low to high, and back on each input transitition. If there is no AC input, both $U1_a$ and $U1_b$ outputs are low. An input voltage of 65 VRMS is made necessary by the voltage dividers R1 and R4 and R2 and R5. As long as the reset input of U2 is held low (no ringing), the chip is allowed to clock at a period of 128 msec. This clocking operation keeps resetting U3, holding its output low. If a ringing signal of proper specs is received, U2 will be reset often enough to keep its output from going high.

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Under this condition U3 is allowed to clock without interference. After 512msec. of ringing, the Q_{10} output of U3 will go high.

If the enable input is low at this time, the circuit is allowed to answer the ring. U4 is clocked by the rising output of U3, and remains latched until the enable line goes high, clearing the flip-flop and dropping the line. The Flip-flop controls K1 which is the seizure relay.

The combination of T1 and R12 provide a 900 Ohm AC and DC impedance, providing the holding resistance without use of a hold coil.

Milliwatt Generator:

This generator consists of a standard wein bridge circuit, with a thermistor in the ~~feedback~~ loop. The thermistor is operated at a bead temperature of approximately 250 degrees C, exhibiting a resistance of 100 Ohms. With the bead at this high temperature, ambient temperature changes cause little effect on the level or freq. stability of the oscillator.

The oscillator output is coupled to the transformer via the driver stage, with the level adjusted by R15.

When adjusting the oscillator, first set the frequency for 1004 Hz + 1 Hz by R19. Then set the level for 0±.1dbm with K1 operated and looking into a 900 Ohm load. (0dBm ± .948 VRMS).

Sleeve Sensor:

A good sleeve in this case will be either an open or a voltage more positive than -5 Volts. This is done so that the sensor may be operated without a sleeve lead attached. A voltage more negative than -12 Volts is considered bad. The region between -5 and -12 Volts can be either good or bad, depending on the direction in which the transition occurred. This is due to hystersis in the sensor, and the voltage divider operation of R20 and R21.

If a sleeve is good, then $U5_d$ will be high. If the jumper is set up for B-C connection, the output line incoming circuit will be low, indicating a good call. In this case, only the sleeve is of interest.

If the A-C jumper is used, the sleeve must be good, and a proper ring received for the incoming circuit line to go low.

All power is brought to the board via the 16 pin flat cable socket. Tip, Ring, sleeve and two spare leads are provided by the barrier strip. Relay K1 can be operated without detecting ring via a line from the flat cable socket.

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		ENGR.	DATE
NEC-100R-0776	INCOMING CIRCUIT	DRAWING NO. 0041-I3-415	REV

41-3A KEYBOARD

A-0041-13-417

I. APPLICABLE DRAWINGS:

B-0041-13-017 Assembly
D-0041-13-317 Schematic
9700-96829 Hole Schedule

II. SCOPE:

This document contains circuit operation, and test requirements for the keyboard alone.

III. GENERAL:

The board actually contains two basic functions; BCD switch interconnect, and Keypad/Q.D. decoding. The BCD switch is composed of seven identical, BCD complement switches. The schematic for the circuit has designations 8, 4, 2, 1, and C on each switch section. The '8' is the most significant bit of the BCD code, while the '1' is the LSB. The 'c' line is normally grounded through pin 11 of the flat cable connector. The following truth table holds true for each switch position and module.

switch module setting	2^3 (8)	2^2(4)	2^1(2)	2^0(1)
0	gnd	gnd	gnd	gnd
1	gnd	gnd	gnd	open
2	gnd	gnd	open	gnd
3	gnd	gnd	open	open
4	gnd	open	gnd	gnd
5	gnd	open	gnd	open
6	gnd	open	open	gnd
7	gnd	open	open	open
8	open	gnd	gnd	gnd
9	open	gnd	gnd	open

The keypad section is comprised of a set of switches, with blocking diodes. The diodes should not exceed 1 volt forward drop at 10 mA forward current. This current should not be exceeded, and the reverse voltage across any diode should not be greater than 20 volts. It will be noticed that the diodes and switches are in groups, with a common

NORTHEAST ELECTRONICS itt CONCORD, NH, U.S.A	DRAWN BY	SCALE
	ENGR.	DATE
41-3A KEYBOARD	DRAWING NO. A-0041-13-417	REV

NEC-100R-0776

line for each group. The diodes are used to keep one switch closure from affecting any other switches within a group. Only one group is accessed at any one time under normal conditions.

Groupings are as follows, by common line:

Line $\overline{\text{sel0}}$ pin 38

KP-1, KP-2, KP-3, KP-4, KP-5, KP-6, KP-7, KP-8

Line $\overline{\text{sel2}}$ pin 12

KP-9, KP-0, KP-WSD, KP-EON

The remaining diodes are connected to quick-disconnect pins usually attached to the Dial Mode switch, and RST-NORM-LOAD switch.

LINE SWITCHING/INTERFACE

A-0041-13-418

I. APPLICABLE DRAWINGS:

B-0041-13-018	Assembly
B-0041-13-318	Schematic
9700-96825	Hole Schedule

SCOPE:

This document provides circuit descriptions and test performance criteria for the board level assembly alone. Descriptions and Specs. are provided for each circuit type as a sub-heading.

II. GENERAL:

The board contains circuits for the following individual functions:

a) Tracetone generator
b) C-Lead buffering
c) Sleeve hold control circuit
d) A-B channel selector
e) MCS connect/disconnect ckt.
f) MCS address drivers

Tracetone Generator:

This circuit is comprised of two CMOS oscillators, one at 1165 ± 500 Hz. This oscillator is gated by a second oscillator at a frequenct of 4 ± 2 Hz. Both oscillator outputs are buffered showing up at Bleep and Bleep Gate, respectively. This generator produces a distinctive tone for easy identification during tracing operations, and it furnishes an alarm signal during a fault.

The $\overline{\text{Bleep}}$ putput is also boosted in level by U2, and transformer coupled to Pins 1 and 2 of the card edge. The output impedance is a nominal 900 Ohms ± 90 Ohms (AC). R26 should be adjusted for peak signal level of 3 Volt p-p, ± .2V p-p terminated into 900 Ohms. In actual use, this output may be terminated by either 900, 450 or 300 Ohms, depending on how much tracing is being done at one time. These loads will naturally drop the output signal level seen on the lines.

C-LEAD BUFFERING

The sleeve leads are buffered and voltage limited on this board before traveling to the C-Lead timing circuits on another board. Channel A (pin H) is buffered to output Pin 12. Channel B (Pin 7) is buffered to output Pin 13.

The inputs are biased to -12 Volts through 100K Ohm resistors. This voltage should appear at the outputs, if the inputs are left open. The output voltage should not go more negative than -12.8V, nor more positive than +0.8 volts, regardless of the input level beyond these limits.

A square wave put into the sleeves should be rounded at the output by the action of C2 and C4. A 0 dBm 1 Khz signal (sine) at the sleeve inputs should result in an output level of approximately -15 dBm. This is only a reference guide to indicate that the capacitors are in the circuit operating as a low pass suppression network.

SLEEVE-HOLD CONTROL

This circuit is a simple level conversion circuit,when a +5 Volt input to Pin 8 will result in a +5 Volt signal output at Pin D. If the input is grounded, the output will be open. This circuit is used to interface a low current CMOS driver to the high current Sleeve Hold Circuit, whose voltage at Pin D may go negative 10 volts.

A-B CHANNEL SELECTOR:

Let us assume that the MCS cutout relay K1 is not energized and the contacts are closed. Then K2 is used to couple pins A,B,C (T_{sel}, R_{sel}, S_{sel}) to either Channel A or Channel B Line Control jacks, or the MCS' lines.

The following table indicates the valid continuity specs under the above conditions:

CHB (Pin V)	CONTINUITY BETWEEN PINS	
GND	A - E - 11 B - F - M C - H - 10 5 - L 6 - 9 7 - K	Assumes K1 not operated Pin J at + 12 Volts
+ 5 Volts	A - 5 - L B - 6 - 9 C - 7 - K E - 11 F - M H - 10	

MCS CONNECT/DISCONNECT

This function is implemented by K1, controlled by input Pin J. A ground on this pin will operate K1, opening the contacts. K1 is not suppressed, so watch what is used to close the contacts. In unit operation the contacts are opened when a plug is inserted in either Channel A or Channel B line control jacks closing a contact in the jack. This is used to keep lines plugged into the front of the unit from connecting to the MCS lines.

PIN J	CONTINUITY BETWEEN (Ignore A-B SELECTOR)
Open or +12 Volts	E - 11 F - M H - 10 5 - L 6 - 9 7 - K
Gnd	All above connectons open

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DRAWN BY		SCALE
ENGR.		DATE
LINE SWITCHING/INTERFACE	DRAWING NO. A-0041-13-418	REV

NEC-100R-0776

MCS ADDRESSING

The address drivers are darlington connected transistors, set up such that +5 volts on the input to a driver will cause the output to go towards ground. Because of the darlington circuit, the lowest output voltage will be approximately 1 volt at 130 Ohms to +12 volts. A ground on the input will cause the output to go to the pullup voltage. These circuits are driven by CMOS outputs and in turn control 12 volt relays with a coil resistance of either 130 or 65 Ohms.

POWER REQUIREMENTS

+ 5 Volts at 10 mA Max.

± 12 Volts at 30 mA Max.

+ 12 Volts at 180 mA Max.

Voltage tolerance ± 5%.

DIALING/HOLDING BOARD

I. APPLICABLE DRAWINGS:

B-0041-13-019	Assembly
D-0041-13-319	Schematic
9700-96814	

SCOPE:

This document provides the circuit design theory, setup and test requirements for the board level assembly.

II. GENERAL

This board is the front-end of the 41-3A system providing DC holding and seizure, as well as the AC balanced line interface. DC line control is accomplished thru the use of an 'active hold circuit'. AC impedance is provided by T1. Loop and leak networks are switched in and out according to control logic provided by the dialer generator/timer board.

The DC hold circuit operates in one of 2 modes;

105 $\pm$ 5 ma hold coil current

open circuit and full current.

The circuit will draw as much current as supplied by the line. The circuit is fused on the board by a .5A fast fuse. The bias voltage for Q8 and Q9 is provided by a floating supply comprised of T2 and associated components. This circuit operates as a high frequency AC-DC converter, with a 1 MHZ input to Pin 4 of the card edge. The bias output voltage is 6.2 Volts ± 5%.

This circuit allows the holding circuit to operate with a high degree of balanced with respect to ground.

The make or break function is controlled by Q6 and U1 an opto-isolator. The circuit is in the break mode when card edge Pin 9 is +5 Volts. This causes Q6 to turn on, keeping Q8-Q9 darlington off.

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	ENGR.	DATE
DIALING/HOLDING BOARD	DRAWING NO. A-0041-13-419	REV 2

NEC-100R-0778

When card-edge Pin 9 is at ground, U1 is turned off. This allows Q8-Q9 and Q6 to turn on.

DC checks should be made in the following manner and order.

1) Strap pins 3 and C.
2) Take Pins 9 and K to gnd.
3) Take Pin 10 to +5 Volts.
4) Supply 48 Volts to (across Pins 1 and A, through a 400 Ohm resistor (10% tolerance and DC current meter),

9) The current reading should now be 115mA ±7mA.
10) Taken Pin 9 to +5 Volts.
11) The current should drop to less than 1mA.

Both the loop and leak networks are bypassed when pin K is at ground and they are in the circuit when the pin is at +5 Volts.

The tip-ring reversal sensor is comprised of U2 and associated diodes. If the loop has current flowing (13mA or more) and pin A is more positive than Pin 1, output Pin 12 will be low if a resistor is tied to ground. If Pin 1 is more positive than Pin A then output Pin 12 will be pulled to +5 Volts. This condition is a tip-ring reversal.

The transformer circuit is cut in or out of the line by card edge Pins 9 and 10. If both are at ground, then the transformer is coupled to the line via C1 and R6. If either input is taken to +5 volts, then the transformer will be off the line.

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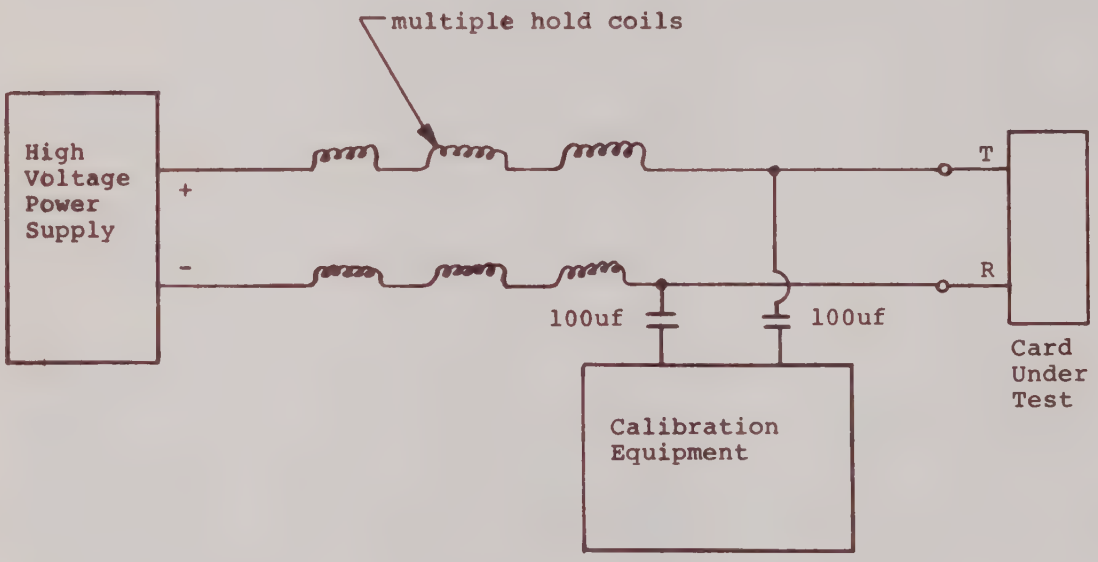
NEC-100R-0776	DIALING/HOLDING BOARD	DRAWING NO. A-0041-13-419	REV 2

The transformer is used both to couple signals into and from the 41-3A and to provide a 735 Ohm AC impedance. All impedance and level adjustments should be made with a wet loop, as below:



The impedance should be adjusted by R5 as follows: set for 740Ω ±1%

Next set up the TT level by applying a 2 Volt ±5 MVOLT RMS signal across Pins 8 & Z, 1 kHz. Terminate Pins A and 1 with 900 Ohms and adjust R25 for a level of -6 dBm ±.1dBm at pins A & 1 900 Ohms reference.

Miscellaneous:

With pin 10 at +5 volts the hold coil (4) is shorted by contact of relay K2.

The pulsing circuit is designed to allow a relay to operate with the least distortion introduced by the dialing circuit. This allows the 41-3A to dial with a high degree of accuracy, comparable to unsuppressed contacts.

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		ENGR.	DATE
DIALING/HOLDING BOARD		DRAWING NO. A-0041-13-419	REV 2

NEC-100R-0776

Page 5

POWER REQUIREMENTS

5 V ± 5% @ 100mA Max.

+12V ± 5% @ 50mA Max.

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		ENGR.	DATE
DIALING/HOLDING BOARD		DRAWING NO. A-0041-13-419	REV O

NEC-100R-0776

DIGITAL TTMF GENERATOR

A-0041-13-420

I. APPLICABLE DRAWINGS:

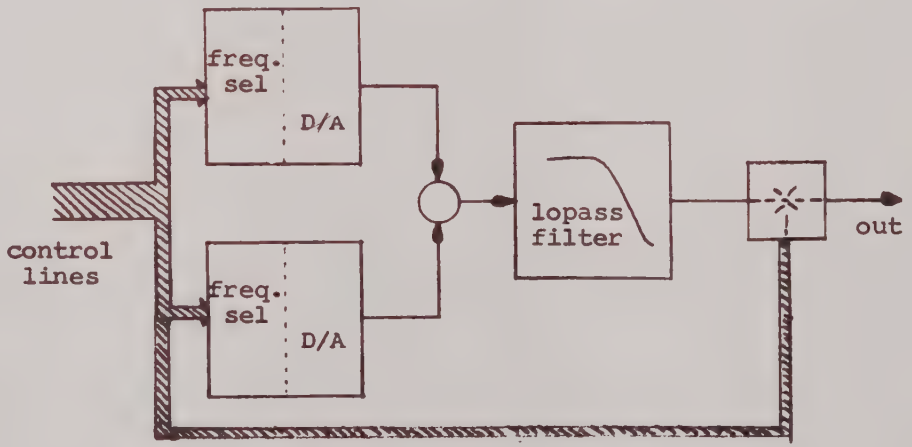
C-0041-13-020 Assembly
D-0041-13-320 Schematic
9700-96825 Hole Schedule
A-0041-13-751 CT-2 Spec
A-0041-13-751 CT-1 Spec

II. SCOPE:

This drawing covers the design theory, and test specifications for the board. Specific use is listed for the 41-3A only, with notes applicable to other uses.

III. GENERAL:

This board uses a digital approach to generate the dual tones required for both Touchtone® and multi-frequency signalling. Frequencies are crystal controlled, either by an on board oscillator, or from an external 1 mHZ source. The board contains two identical oscillator circuits, and a low-pass filter output stage. The sine waves are derived from a stepped current source, and smoothed by the filter.



Overall Block Diagram

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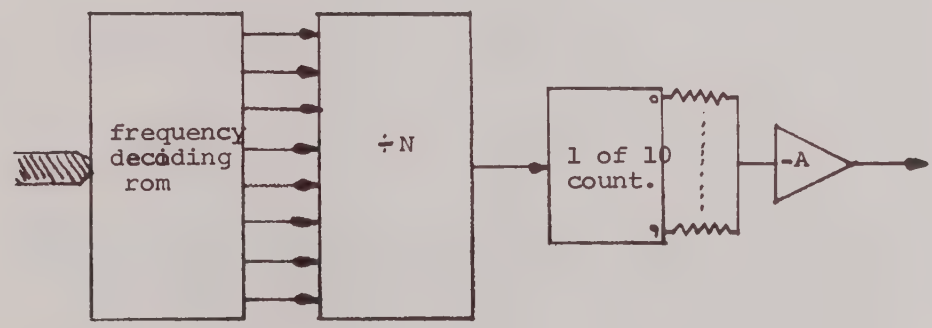
		ENGR.	DATE
DIGITAL TTMF GENERATOR		DRAWING NO. A-0041-13-420	REV

NEC-100R-0776

Basic Oscillator

Each oscillator is nearly identical, the only difference being the ROM that controls its' frequency. The basic frequency of the board is a 1 mhz reference. This is divided by the programmable dividers according to the ROM output. The dividers are an 8 bit string, with a capability to divide from 2_{10} to 255_{10}. Since the sine is generated by a ten step counter, the desired output frequency is multiplied by ten, to get the F_{shift} frequency. The desired divider value (base 10) is found by dividing the desired F_{shift} into the 1 mhz base frequency. The resulting division must be rounded. It should be noted that as the division ratio becomes smaller, i.e., as output frequency gets larger, the error produced by rounding increases. For this reason, the 2600 and 2400 hz outputs are in error by more than 1%.



Oscillator Block Diagram

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		ENGR.	DATE
DIGITAL TTMF GENERATOR		DRAWING NO. A-0041-13-420	REV

NEC-100R-0776

The sinewave is generator by the counter, which sources current through one resistor at a time into the op-amp. Each resistor is a weighted value, determined to give the proper sine value for that position on a curve. Since all input values are positive, the output of the op-amp will be negative at all times. This output is capacitively coupled into the output filter.

The filter is a modified biquad, with a chebychev response, 4 pole. It is required to eliminate the harmonic content of the stepped sine generated by the op-amp. It is able to reduce the total harmonic distortion (THD) to below 4% for the 700 hz frequency, and nearer 1% for the highest frequency, 2600 hz.

The output of the filter can be gated by K1, under control from the input pins.

The 1 mhz reference frequency is provided by the mainframe in the 41-3A system, although circuitry is provided for on-board sourcing. This circuit is not loaded in the 41-3A system, and the strap is not connected. The oscillator (1 mhz) is not critical of crystal type, and fine-tuning is not necessary for this application.

More data on the design and calculations for the filter stage can be found in the appendix to this document.

The card may be tested completely by manipulating the eight Address lines (TTMF7-TTMF0), and TTENABLE, and MFENABLE.

TTENABLE, MFENABLE, and TTMF7 are used to control relay K1. A high (+5) on any of these lines will close K1, bringing the filter output to pin 64 on the card edge.

The other address lines are used to change the frequency of each oscillator, and control the enabling of each oscillator. TTMF6, when taken high, disables the oscillator comprised of counter U10, controlled by U1 (labelled CT-2). TTMF5 controls the other oscillator in a similar manner. The lines enable the oscillators when taken low to ground.

TTMF4 is part of the 5 bit frequency select address. This line determines whether TT or MF tones will be generated by the oscillators. A high will select MF outputs, a low selects TT frequencies in general. If the TTMF7, TTENABLE, or MFENABLE line is taken high, and the following truth tables used, the card should generate the indicated frequencies on a single tone basis for test. Distortion should be less than 4%.

NORTHEAST ELECTRONICS inc CONCORD, NH, U.S.A.		DRAWN BY	SCALE
		ENGR.	DATE
NEC-100R-0776	DIGITAL TTMF GENERATOR	DRAWING NO. A-0041-13-420	REV

Page 5

TRUTH TABLE I

CT1 ROM

Correct test freq. ±1 hz

TTMF6	TTMF5	TTMF4	TTMF3	TTMF2	TTMF1	TTMF0	Output	Frequency
1	0	0	0	0	0	1	697	699
1	0	0	0	0	1	0	697	699
1	0	0	0	0	1	1	697	699
1	0	0	0	1	0	0	770	769
1	0	0	0	1	0	1	770	769
1	0	0	0	1	1	0	770	769
1	0	0	0	1	1	1	852	855
1	0	0	1	0	0	0	852	855
1	0	0	1	0	0	1	852	855
1	0	0	1	0	1	0	941	943
1	0	1	0	0	0	1	700	699
1	0	1	0	0	1	0	700	699
1	0	1	0	0	1	1	900	901
1	0	1	0	1	0	0	700	699
1	0	1	0	1	0	1	900	901
1	0	1	0	1	1	0	1100	1099
1	0	1	0	1	1	1	700	699
1	0	1	1	0	0	0	900	901
1	0	1	1	0	0	1	1100	1099
1	0	1	1	0	1	0	1300	1299
1	0	1	1	0	1	1	1100	1099
1	0	1	1	1	0	0	1500	1493
1	0	1	1	1	0	1	700	699
1	0	1	1	1	1	0	900	901
1	0	1	1	1	1	1	1300	1299
1	0	0	1	0	1	1	941	943
1	0	0	1	1	0	0	941	943

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DIGITAL TTMF GENERATOR

DRAWING NO. A-0041-13-420

REV

NEC-100R-0776

TRUTH TABLE II

CT2 ROM

Correct test freq/±1 hz

TTMF6	TTMF5	TTMF4	TTMF3	TTMF2	TTMF1	TTMF0	OUTPUT	FREQUENCY
							1209 hz	1205
0	1	0	0	0	0	1	1336	1333
0	1	0	0	0	1	0	1477	1471
0	1	0	0	0	1	1	1209	1205
0	1	0	0	1	0	0	1336	1333
0	1	0	0	1	0	1	1477	1471
0	1	0	0	1	1	0	1209	1205
0	1	0	0	1	1	1	1336	1333
0	1	0	1	0	0	0	1477	1471
0	1	0	1	0	0	1	1336	1333
0	1	0	1	0	1	0	900	901
0	1	1	0	0	1	1	1100	1099
0	1	1	0	0	1	0	1100	1099
0	1	1	0	0	0	1	1300	1299
0	1	1	0	1	1	0	1300	1299
0	1	1	0	1	0	1	1300	1299
0	1	1	0	1	1	0	1500	1493
0	1	1	1	0	0	0	1500	1493
0	1	1	1	0	0	1	1500	1493
0	1	1	1	0	1	0	1500	1493
0	1	1	1	0	1	1	1700	1695
0	1	1	1	1	0	0	1700	1695
0	1	1	1	1	0	1	2400	2381
0	1	1	1	1	1	0	2600	2632
0	1	0	1	1	1	1	1209	1205
0	1	0	1	1	0	0	1477	1471
0	1	1	1	1	0	1	1700	1695
0	1	1	1	1	1	0	1700	1695
0	1	1	1	1	1	1	1700	1695

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	ENGR.	DATE
DIGITAL TTMF GENERATOR	DRAWING NO. A-0041-13-420	REV

NEC-100R-0776

The oscillators may be tested individually as in the previous tables, or in combination. The following truth table gives the address, and resulting output keycode that will result.

TTMF4	TTMF3	TTMF2	TTMF1	TTMF0	frequencies	code
0	0	0	0	1	1209 697	tt-1
0	0	0	1	0	1336 697	tt-2
0	0	0	1	1	1477 697	tt-3
0	0	1	0	0	1209 770	tt-4
0	0	1	0	1	1336 770	tt-5
0	0	1	1	0	1477 770	tt-6
0	0	1	1	1	1209 852	tt-7
0	1	0	0	0	1336 852	tt-8
0	1	0	0	1	1477 852	tt-9
0	1	0	1	0	1336 941	tt-0
0	1	0	1	1	1209 941	*
0	1	1	0	0	1477 941	#
1	0	0	0	1	900 700	mf-1
1	0	0	1	0	1100 700	mf-2
1	0	0	1	1	1100 900	mf-3
1	0	1	0	0	1300 700	mf-4
1	0	1	0	1	1300 900	mf-5
1	0	1	1	0	1300 1100	mf-6
1	0	1	1	1	1500 700	mf-7
1	1	0	0	0	1500 900	mf-8
1	1	0	0	1	1500 1100	mf-9
1	1	0	1	0	1500 1300	mf-0
1	1	0	1	1	1700 1100	KP
1	1	1	0	0	1700 1500	ST
0	1	1	1	0	2400	SF-1
0	1	1	1	1	2600	SF-2
1	1	1	0	1	1700 700	ST3P
1	1	1	1	0	1700 900	STP
1	1	1	1	1	1700 1300	ST2P

OUTPUT:

a) level 2 volts RMS ±.12 volts (single tone)

b) distortion less than 4% (single tone)

ANALOG DETECTOR/MONITOR

A-0041-13-421

I. APPLICABLE DRAWINGS:

C-0041-13-021
D-0041-13-321
9700-96830

II. SCOPE:

The Analog Detector board is the heart of the 1 khz, and low tones detection, and therefore should be set up with care. This specification provides the operating theory and test requirements, as well as specific methods and equipment for setting this board up. Once set up, this board should require no further adjustment in the overall unit.

III. GENERAL:

This board provides the following general functions;

1 khz detector

lo tones detector

monitor amplifier

sleeve hold control, hold current level control

The monitor section contains switching circuitry to control the signal direction, enable and disable detectors and monitor inputs, and provide the sleeve and current controls. These switching circuits may be checked out in the following manner.

Turn R34 and R35 clockwise approx. 10 turns.

Apply a 1 khz signal (0 dbm) to card edge pins 63 and 64.

The signal should be seen at TP-1 if card edge pins 81 or 82 are taken to ground, and only under these conditions.

The signal should be seen at TP-2 if card edge pins 78 or 81 are taken to ground, and only under these conditions.

The signal should be seen at card edge pin 58 if card edge pins 83, 78, 81, or 82 are taken to ground. The amplitude signal should be controlled by the 'master volume' control attached to pins 1, 3, 5. The amplitude should not be affected by the 'dialing volume' control on pins 2, 4, 6. Both of these pots must be 50K nominal resistance.

The signal should be seen at card edge pin 58 if card edge pin 79 is grounded, and the amplitude should be controlled by the

NORTHEAST ELECTRONICS Int CONCORD, NH, U.S.A.	DRAWN BY	SCALE
	ENGR.	DATE
ANALOG DETECTOR/MONITOR	DRAWING NO. A-0041-13-421	REV

NEC-100R-0776

'dialing volume' control, and not affected by the 'master volume'.

If card edge pin 56 is grounded, the signal should not be seen at card edge pin 58 under any of the above conditions.

If a 1 khz square wave (TTL level) is presented to card edge pin 96, it should be seen at card edge pin 58 when card edge pin 83 is grounded. The amplitude may be controlled by R36, and should be set to maximum amplitude.

If the above tests worked out ok, then the signal switching section of the circuit works. The next tests concern the monitor amplifier itself, and the sleeve hold, and current level outputs.

Sleeve hold disable output pin 61 should be high if input pins 77, 78, or 84 are grounded. This output is CMOS, and should not be loaded with less than 22k ohms. A high will be +4 to +5 volts dc.

Hold current seizure output pin 60 will be low if pinput pins 81, or 82 are grounded. This is also a CMOS output, and should not be loaded with less than 22k ohms.

The monitor amplifier should perform as follows (or at least attempt to), with a 45 ohm speaker load from card edge pin 58 to ground. Card edge pin 78 should be grounded, and the master volume set for max (short pins 3 to 5). The frequency/amplitude response of the monitor should be as follows, for an input amplitude of 474 mv rms.

freq. (hz)	output (vrms)	limits (vrms)
60	≥7.0v	
200	7.5	1.25
400	7.0	
600	6.0	
800	5.0	
1000	4.0	
1400	3.0	
1800	2.25	

1 KHZ DETECTOR ALIGNMENT

The 1 khz detector consists of a two-stage biquad bandpass filter, with frequency adjustments, and a precision rectifier (average), followed by a DC comparator circuit for limit detection. The filter is tuned such that the first stage peaks at 990 hz, and the

second stage peaks at 1020 hz, providing a steep skirt bandpass filter.

Card edge pin 81 grounded, input level to pin 63 should be .474 v rms ±.005 v rms) output observed at TP-4. The output level of the filter will be unspecified, and the db drops are referenced to this drop.

Tuneup is as follows:

set frequency to 990 hz ±hz, adjust R39 for a peak reading at TP-4. Set frequency to 1020 hz ±1 hz, adjust R47 for a peak reading at TP-4.

The overall frequency response of the filter should be something like the following table:

frequency(hz)	drop from peak(1004 hz)	limits
400	65 db	5 db
600	56	5
800	41	5
900	28	3
950	17	3
990	1	1
1000	0	.5
1010	0	.5
1020	1	1
1050	13	2
1100	25	3
1200	37	3
1500	51	3
1600	54	4

The threshold detectors, and average detector should be aligned in the following manner:

1. Ground TP-7 to the center ground on the board. With a DVM, look at TP-10 (dc scale), and adjust R83 for 0v ±5 mv dc offset. Release the ground from TP-7.

2. Look at TP-6 with the DVM (dc scale), and adjust R62 for 3.000 volts dc, ±1 mv.

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	ENGR.	DATE
ANALOG DETECTOR/MONITOR	DRAWING NO. A-0041-13-421	REV

NEC-100R-0776

3. Apply a 1004 hz, 1.500 vac rms signal to edge pin 63. Ground pin 81, and adjust R34 for approximately 7.84 ±10 mV vdc, at TP-5. Record the dc reading at TP-5. Reset the input level to 15 mv rms, a 40 db drop. Observe the reading at TP-5, and adjust R59 such that the reading is 40 db lower than the pervious measurement.

4. Repeat step 3 until a 40 db input change results in a 40 db dc change, ±3 mv dc.

5. Set the input level to 15 mv ac rms, and adjust R34 for a dc voltage of 78 mv dc, at TP-5.

The threshold adjustments are now complete for the 1 khz detector, and we will now move on to check the min/max threshold detectors.

Do not put any signal into the board, and look at card edge pin 25. It must be high (external +5 pullup required). Now put a 1004 hz, 11 mv ac rms signal into pin 63, with pin 81 grounded. Output pin 25 should still be high. Slowly adjust the input level until pin 25 goes low, and observe input level. This should be between 12 mv, and 15 mv rms. Remove the signal, and the output should go high. Upon reapplication of the signal, there should be a 2 second (± 1 sec) delay until the output pin goes low.

Put a 13.886K ohm, ±1% between card edge pins 41 and 45.

Put a 2.654K ohm, ±1% between card edge pins 47 and 49. This sets the unit up for ±1 db limits.

Put a 554 ohm, ±1% resistor between card edge pins 39 and 43. This is the EML position, 0 dbm range. Apply a 474 mv rms ac signal to pin 63, and observe that neither the hi level (pin 27), nor the lo level (pin 23) outputs go low. These outputs must be pulled up to +5 volts. Adjust the signal input upwards until the hi level goes to ground. The input level should be between 502 mv rms, and 563 mv rms. This provides an accuracy of .5 db for the hi level detector.

Now adjust the input level downwards until the lo level line goes to ground. The input level should be between 447 mv rms, and 399 mv rms. This is for .5 db accuracy on the lo level detector.

Now change the resistor between pins 39 and 43 to an open circuit and look for a high level indication. The input reading should be between 50 mv rms, and 56 mv rms. Next look for a lo level indication, the reading should be between

45 mv rms, and 40 mv rms. This just checked out the variable gain stage of U12.

The card should not be able to give either a high or low indication until it gives a 1 khz present indication, a low on pin 25.

Low Tones Detector Alignment

This filter and detector is used to detect the presence of tones in the range of 200 to 650 hz, typically used in the busy, reorder, and dialtone generators. The detector consists of a bandpass filter, and an average detector after it. The DC voltage from the avg detector drives a simple threshold comparator that hauls its reference up with it, and looks for crossing of this threshold. This is variable to allow for noise, and is an attempt to average out signal level. It should be noted that due to leakage, at low signal levels, an increase in level will not always maintain a low on the $\overline{\text{mark}}$ line forever, since the following threshold will come up to the main input level after a time. The time is sufficient, however, to recognize dialtone with a level of greater than -30 dbm (900 ohms), and there is no problem with busy or reorder, due to the repetition rate.

The filter may be checked by placing a ground on pin 81, and applying a 474 mv rms signal to pin 63. R35 should be cranked in a clockwise direction about 10 turns. The output of the filter may be observed at TP-11, and the reading in the following table are referenced to this output for a normalized frequency of 400 hz.

frequency	attentuation (db)	limits (db)
60	47	5
200	0	2
500	0	2
600	3	1.5
800	25	3
1000	39	4

Assuming that the filter is working, the loss through the filter should not be set up to match the 1 khz filter loss. Set the input frequency to 1004 hz, 474 mv rms, ground pin 81, and measure the level at TP-4 (ac scale). Remember it.

Now set the frequency to 404 hz, same level. Measure the ac level at TP-11, and adjust R35 so that this level matches that measured at TP-4. With this accomplished, the EML stage can now be used to look at NNX-1-NNX tones in some special offices. The switch (S49) is used for this distinction. It might be noted here that in all previous operations, this switch was in the 1 khz position.

The next step is to adjust the low tones detector threshold. First adjust R114 fully clockwise (approx 20 turns). Apply a 404 hz, 15 mv ac rms signal to card edge 63. Observe output pin 25 (card edge, +5 ext pullup required). Adjust R106 such that with pin 25 high, R106 may be turned to the point that pin 21 goes low. The mark should go low for a 15 mv signal, but should remain high for an 11 mv rms signal, or less. Any signal higher than 13 mv should hold the mark lead low.

The board is now ready to ship but don't forget to glyptol all the adjustments.

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ANALOG DETECTOR/MONITOR	DRAWING NO. A-0041-13-421	REV 1

NEC-100R-0776

DIAL GENERATOR/TIMER

A-0041-13-422

I. APPLICABLE DRAWINGS:

C-0041-13-022 Assembly
D-0041-13-322 Schematic
9700-96824 Hole Schedule

II. SCOPE:

This document contains circuit descriptions, test requirements and techniques for the card. This card provides the main timebase and timing functions for the 41-3A system.

III. GENERAL:

This card can be broken down into the following general circuits:

a) Main Timebase Generator

b) Dial Speed Generator

c) % Break Generator

d) Interdigital Timer

e) Front Panel System Timers

f) Dialer Control Logic

g) C-Lead Timers

h) Tip-Ring Reversal Timer

These circuits are mainly CMOS, except those required to operate at high speeds. Logic probes should be used with caution, since there are some chips that operate at voltages other than ground and +5 volts. All testing can be done from the card edge connector, eliminating the need for pressure pins. Due to the density of the board, test points are not provided on Q/D pins or similar.

Test procedures and suggestions, as well as specs will be contained in the body of the circuit descriptions that follow in a Functional breakdown basis.

NORTHEAST ELECTRONICS nt CONCORD, NH, U.S.A	DRAWN BY	SCALE
	ENGR.	DATE
DIAL GENERATOR/TIMER	DRAWING NO. A-0041-13-422	REV

NEC-100R-0776

Main Timebase Generator

The main timebase is a crystal controlled oscillator operating at 10 MHZ. This frequency is divided several times to provide 1 usec, 10 usec, 100 usec, 1 msec, and 10 msec outputs (±.01%). The outputs are pulses not necessarily square (50% dutycycle) waves. These functions are provided by U15, U10, U12, U13, and U23. The outputs are CMOS buffered, with a load capability of 2 TTL loads each. The logic levels are gnd and +5 volts. These outputs are running all the time that power is applied to the card.

Dial Speed Generator

The heart of the dial speed generator is the two digit rate multiplier, U6 and U7. These chips are connected such that for each 100 input pulses from U15, they will only put out a percentage of them, according to the setting of the dial speed switches, as follow:

$$P_{out} = \frac{(MSD)\ (LSD)}{100}$$

The output pulses are not evenly spaced, but may occur in clumps, depending on the switch setting. For this reason, the output is divided by 1000, which reduces the apparent phase jitter by 60 dB. It also reduces the frequency by 1000. The output of U14 is now nice and even, with no visible jitter. This output will feed the % Break circuit. Note that the speed dividers is controlled by the dialing ($\overline{S2}$) input line. A low on this line will allow the circuit to operate, while +5 volts will shut it down.

% Break Generator

The generator consists of two BCD counters, and two BCD comparators. The counters are clocked by the output of U14, and are enabled by a low on the dialing ($\overline{S2}$) line. The counter outputs feed a pair of comparators, whose other inputs are the % break switches. The output of the A<B pin of U8 will be high and low according to the setting of the switches. A low on this output is the MAKE portion of a dial pulse. This output may have some very narrow (a few nanoseconds) pulses on it due to internal timing, which can foul up the dial digit counter. This is eliminated by feeding the signal into the reset input of a shift register which is clocked at a 1 usec rate. This register, U17, assures that a valid level (low) is more than 4 usec wide. The output of the register is then fed into the dialed digit counter. This would create an error in the % break output, except that the signal fed to the dialer control circuitry does not have the protection circuit, since the rest of the world can't respond to pulses of such narrow width.

The dialed digit counter is used by the processor to signal the end of a dial pulse digit. The processor feeds the counter (U16) a BCD code for the number of pulses to be dialed. The digit is jammed in while the dialing (s2) line is high. When the s2 line goes low, the counter is allowed to clock. Once it has counted down to zero, its carry out output will go low, indicating to the processor that the digit is finished. Note that this output also has a shift register verifier on it. The chip used in this circuit (U16) is prone to produce very short false carry-out signals, but they are enough to screw up the processor, causing errors in the dialed digit. U15 requires that the carry-out be low for 4 usec, and if it is, the transition is latched into the other half of the chip, to be reset when the s2 line goes high again under processor control. The BCD codes presented to the digit counter are normal, except that the digit '0' must be presented as a binary ten.

Dialer Control Logic

The control logic is used to operate the circuits on the active front end board and dialer. They are combination logic as follows:

- pulsing (70)= [DP mode (47)] · [$\overline{\text{dialing}}$ (79)]
- $\overline{\text{pulsing}}$ (69) is an inversion of pulsing (70)
- The brk line (68) will be high if,
  $\overline{\text{idle}}$(77) + $\overline{\text{recycle}}$(84) + [$\overline{\text{dialing}}$(79) • DPmode(47)•break(U8.12)]
- $\overline{\text{TT Enable}}$(72)=$\overline{\text{dialing}}$(79)·break(U8.12)·TT mode(46)
- $\overline{\text{MF Enable}}$(71) $\overline{\text{dialing}}$(79)·break(U8.12)·MF mode(45)
- Inc rst(74)=$\overline{\text{wsd}}$(78) + $\overline{\text{recycle}}$(84) + $\overline{\text{idle}}$(77) + $\overline{\text{dialing}}$(79)

Interdigital Timer

The timer consists of presettable down counters U1, U2, and U3, as well as part of U17. While the $\overline{\text{idp}}$ line (pin 80) is high, the switch inputs to the counters are jammed into the counters, and the $\overline{\text{carryout}}$ of U1 is high. When the $\overline{\text{idp}}$ line goes low, the counters decrement at a 1 msec rate until they reach zero. At this time, the $\overline{\text{carryout}}$ of U1 goes low, allowing U17 to clock. 4 usec later, the output of U17 will go high, and the END ID line (39) will go high, signalling the end of the interdigital period. U17 is used to inhibit the short carryout spikes generated by the down counters. If the $\overline{\text{idp}}$ line is maintained low, the jammed values have no effect after the counters have reached zero the first time. Thereafter, they will pulse out at a 1 hz rate from the carryout.

NORTHEAST ELECTRONICS inc CONCORD, NH, U.S.A	DRAWN BY	SCALE
	ENGR.	DATE
DIAL GENERATOR/TIMER	DRAWING NO. A-0041-13-422	REV

NEC-100R-0776

Front Panel Timers

Each of the front panel timers operates in the same manner, although some components are different. Each section of U30 is a schmitt trigger inverter operated as an oscillator. The frequency of oscillation is determined by the front panel control potentiometer associated with it. Max pot value is 100k ohms ±10%. Each timer has a control lead, that when taken from gnd to +5 volts allows the counter to run. When the counter has reached the required count, its output goes high. This if fed back to the oscillator via a diode, which stops the oscillator. The counter output remains latched until the endable line goes low again.

The time from enabling the timer to when the output goes high can be roughly calculated as below:

$$T = 2^{Q-1} \times (.693)(R_{ext} + RA + 2RB)(C)$$

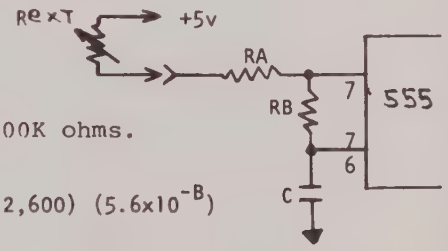
where:

R_{ext}, RA, RB in ohms

C is value of associated cap in farads

Q is output number of the counter chip

T is in seconds



example:

Delay timer if R_{ext} is 100K ohms.

$$T = \left[2^{(12-1)}\right](.693)(100{,}000+12{,}600)\ (5.6\times10^{-B})$$

T = 8.95 seconds

The following table gives expected time durations for each timer. Values have a 15% tolerance. At $R_{ext}=0$, 25% tolerance at R_{ext}=100K.

TIMER	$R_{ext}=0$	R_{ext}=100K (±5%)
Delay start	1 sec	8.95 sec
Dialtone dly	1.24 sec	7.91 sec
Net Dly	5.79 sec	57.46 sec
Test OK	.41 sec	10.06 sec
Recycle	1 sec	8.95 sec

NORTHEAST ELECTRONICS int CONCORD, NH, U.S.A.	DRAWN BY	SCALE	
	ENGR.	DATE	
DIAL GENERATOR/TIMER	DRAWING NO. A-0041-13-422	REV 1	

NEC-100R-0776

If the output of an oscillator is observed, it may be seen to jitter. This is caused by the resistor between the capacitor and the inverter input. This resistor is needed to limit the current pulled from the counter output when the diode is turned on. If the resistor is too small, the risetime of the counter output will be affected.

C-Lead Timers

The C-Lead timers are fixed duration timers employing a counter, and a self-latching circuit. The input to each timer is a CMOS schmitt trigger. Channel A will serve as an example.

The input is on the S line. The voltage limits are -6v and -12 volts. NOTE: Use a series R of 10k when testing the circuit to keep diode currents to safe regions. It will be noticed that the schmitt trigger (U36) operates between -12 volts and -6 volts, so watch out with logic probes.

If the input is at -6 volts, the output of the trigger will be at -12 volts. This will hold Q1 off, keeping U33 reset. The $\overline{\text{Search A}}$ line will be at ground. When the input sleeve goes to -12 volts, Q1 will turn on, allowing U33 to count. $\overline{\text{Search A}}$ will be high. When U33 has counted 512 msec, its output will go high, causing $\overline{\text{SAI}}$ to go low. Also, the clock to the counter will be inhibited by U38, causing the circuit to latch. This is the IDLE condition. If the sleeve reverts to -6 volts, the circuit will be reset immediately. The Channel B. timer operates in the same manner. The output logic levels are gnd and +5 volts, Cmos.

Tip-Ring Reversal Timer

This timer operates in basically the same manner as the C-Lead timers. If pin 73 is at ground, the counter is held reset, and the rev line (37) is low. When the input goes to +5 volts, the timer is allowed to clock. After 128 msec, the REV line will go high, and the counter will be latched until the input goes back to gnd. A high on the REV line indicates a tip-ring reversal.

Power Requirements:

+5 volts at 200 mA, max

-12 volts at 10 mA, max

+12 volts at 10 mA, max

Card Size:

6 x 8 inches, dual 50 pin edge connector, .125 centers.

NORTHEAST ELECTRONICS inc CONCORD, NH, U.S.A.	DRAWN BY	SCALE
	ENGR.	DATE
DIAL GENERATOR/TIMER	DRAWING NO. A-0041-13-422	REV

NEC-100R-0776

SYSTEM I/O BOARD

A-0041-13-423

I. APPLICABLE DRAWINGS:

D-0041-13-323 Schematic
C-0041-13-023 Assembly
9700-96818 Hole Schedule

II. SCOPE:

This document covers the operation, circuit design theory, and test requirements of the system I/O Board. The use of a computer controlled test setup is highly recommended, in view of the large number of input-output lines and combinations.

III. GENERAL:

This board provides the interface between the high speed microprocessor bus, and the rest of the system boards in the 41-3A. It also provides part of the non-multiplexed display drive in the line status section.

The operation of the 8255 PPI devices is discussed more fully in the appendix, abstracted from the INTEL data book. This board contains two PPI devices, providing three 8-bit output ports, one 4-bit output port, one 4-bit input port, and two 8-bit input ports. To successfully access a port, the I/O line must be high. Port assignments and addresses are as follows, with the addresses in hexadecimal format.

Port Label	Address	Type
TTPRT	08	output
TIMST	09	output
DPORT	0A	upper 4 bit input lower 4 bit output
CONT3	0B	control port (88 initialize)
STATP	0C	output
TOUTS	0D	input
DTCTP	0E	input
CONT4	0F	control port (8B initialize)

I. TTPRT is used to provide control codes for the TTMF generator board. The PPI outputs go directly to the card edge, and are able to drive one TTL load each, with a max low level of .4 volts.

NORTHEAST ELECTRONICS int CONCORD, NH, U.S.A	DRAWN BY		SCALE
	ENGR.		DATE
SYSTEM I/O BOARD	DRAWING NO.	A-0041-13-423	REV

NEC-100R-0776

II. TIMST provides control for the five variable timers in the 41-3A, as well as controlling the type of dialing employed for the call. This output port is also able to handle one TTL load per line.

III. DPORT is a split port, with the upper 4 lines (C7-C4) being programmed as inputs. These lines are the test/trace switches in the line unit. The lower 4 bits are an output port used to determine the number of dial pulses for each digit dialed. These lines can handle one TTL load each.

IV. CONT3 is the control port for the above three ports, and must be the first port addressed and written into on this chip. An 88 hex is written to it, setting up the ports for their desired operating characteristics.

V. STATP is an output port, of which only 5 lines are used. The lower 4 bits are used to control a 4 to 16 line decoder, which provides 16 mutually exclusive active low outputs for hardware state control. Each of the state lines can handle 16 TTL loads. The following truth table relates the data written to STATP, and the resulting state line outputs.

STATP	$\overline{S0}$	$\overline{S1}$	$\overline{S2}$	$\overline{S3}$	$\overline{S4}$	$\overline{S5}$	$\overline{S6}$	$\overline{S7}$	$\overline{S8}$	$\overline{S9}$	$\overline{S10}$	$\overline{S11}$	$\overline{S12}$	$\overline{S13}$	$\overline{S14}$	$\overline{S15}$
0000	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0001	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0010	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0011	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0100	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0101	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0110	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0111	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
1000	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
1001	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
1010	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
1011	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
1100	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1101	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1110	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
1111	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

The 5th bit, A_4, is used to determine the channel accessed by the software for sleeve lead sensing during line searches.

NORTHEAST ELECTRONICS int CONCORD, NH, U.S.A	DRAWN BY	SCALE	
	ENGR.	DATE	
SYSTEM I/O BOARD	DRAWING NO. A-0041-13-423		REV

NEC-100R-0776

A '1' will be for channel B, a '0' for channel A.

VI. TOUTS is an input port used to poll various timer outputs. All are true positive logic (active high).

VII. DTCTP is an input port, with the upper 6 bits being true positive, the lower two bits multiplexed by the CHB line of STATP. The $\overline{SAI}$, $\overline{SBI}$, $\overline{SEARCH\ A}$, and $\overline{SEARCH\ B}$ lines are switched into these two lines according to the following table.

				chb 0		chb 1	
$\overline{SAI}$	$\overline{SBI}$	$\overline{SEARCH\ A}$	$\overline{SEARCH\ B}$	C1	C0	C1	C0
0	0	0	0	1	0	1	0
0	0	0	1	1	0	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	1	1
0	1	0	0	1	0	0	0
0	1	0	1	1	0	0	1
0	1	1	0	1	1	0	0
0	1	1	1	1	1	0	1
1	0	0	0	0	0	1	0
1	0	0	1	0	0	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	1	1
1	1	0	0	0	0	0	0
1	1	0	1	0	0	0	1
1	1	1	0	0	1	0	0
1	1	1	1	0	1	0	1

Interrupt Circuitry

In the 41-3A System, there are ten interrupts available:

one for the TTYY acia,
five for the asynchronous timers, individually cleared by the servicing routine they report to.
End Delay Start
End Dialtone Delay
End Network Delay
End TOK period
End Recycle period
Four are synchronous with the system clock, and are cleared and serviced immediately by the ISR routine in the software.

End Digit ↑
End Interdigital Period ↑
10 Msec clock ↑
1 Msec clock ↓

The arrows indicate the transition causing an interrupt. These interrupts must be recognized immediately, and then cleared out so that they don't tie up the system. Flipflops U4 and U5 are used to provide the edge sensitivity, and U12 and U13 provide steering the the reset action (under software).

U14 and U15 combine the 9 system interrupts into a common request line, INTR, which will go low to request an interrupt service.

The RST line is used initially to clear the PPI's, and the four interrupt flipflops. The TINT address (10 hex) is used to clear the interrupt flipflops after a request has been made, and the requesting device identified by the software.

Line Disposition Circuit

U17, 18, 19, 20, 6, and 21 are used to combine the test, trace, sleeve sensor, and state lines. These lines are decoded to drive the line status lamps in the line display area. The following truth table gives the test parameters. It must be noted that the chb output (pin 98) is important to the table. The flipflop D input is controlled from the STATP. When this input line is high, channel B is indicated, and will be latched in by a rising edge of the $\overline{S0}$ input. A low will indicate channel A. This must be done if the UTAL and UTBL table entries are to be correct.

Page 6

$\overline{TRC\ A}$	$\overline{SAI}$	$\overline{TRC\ B}$	$\overline{SBI}$	$\overline{S0}$	$\overline{S7}$	CHB	$\overline{tral}$	$\overline{idlal}$	$\overline{bsyal}$	$\overline{trbl}$	$\overline{idlbl}$	$\overline{utal}$	$\overline{utbl}$	$\overline{bsybl}$
0	x	0	x	x	x	x	0	1	1	0	1	x	x	1
1	1	0	x	x	x	x	1	1	0	0	1	x	x	1
1	0	0	x	x	x	x	1	0	1	0	1	x	x	1
0	x	1	1	x	x	x	0	1	1	1	1	x	x	0
0	x	1	0	x	x	x	0	1	1	1	0	x	x	1
x	x	x	x	1	1	0	x	x	x	x	x	0	1	x
x	x	x	x	1	1	1	x	x	x	x	x	1	0	x
x	x	x	x	0	1	x	x	x	x	x	x	1	1	x
x	x	x	x	1	0	x	x	x	x	x	x	1	1	x
x	x	x	x	0	0	x	x	x	x	x	x	x	x	x

'x' is a don't care function

NORTHEAST ELECTRONICS int CONCORD, NH, U.S.A.	DRAWN BY	SCALE
	ENGR.	DATE
SYSTEM I/O BOARD	DRAWING NO. A-0041-13-423	REV

NEC-100R-0776

Page 7

Power Requirements:

+5v (±5%) at 300 mA.

NORTHEAST ELECTRONICS int CONCORD, NH, U.S.A.	DRAWN BY	SCALE
	ENGR.	DATE
SYSTEM I/O BOARD	DRAWING NO. A-0041-13-423	REV

NEC-100R-0776

DISPLAY I/O BOARD

I. APPLICABLE DRAWINGS

C-0041-13-024	Assembly
C-0041-13-324	Schematic
9700-96819	Hold Schedule

SCOPE:

This document provides pertinent circuit descriptions, operating, and required test procedures for a board level test and setup.

II. GENERAL

This board provides the interface circuitry between the CPU and most of the front panel and display. A similar board, the SYSTEM I/O Board provides the rest of the interface.

The board basically consists of two Programmable Peripheral Interface (PPI) IC's and associated addressing, and drive circuitry. The processor is able to address ports of each chip, read or write to them. The PPI chips U1 and U2 are very powerful in that they are accessed just like memory by the processor and automatically latch the data written into them. This data may be nondestructively read by the processor so that the PPI's also set as memory saving valuable RAM in the processor section.

To operate the board correctly, the PPI's must be initialized by the processor. This initialization will set up,internally in the chip, just how it is going to be operated and which lines are input and output.

All input/output is 5 Volt logic.

Each chip consists of a processor bus side with an 8-bit bi-directional data bus and address and chip select inputs. The 'system' side of the chip consists of three ports (8 lines each) as follows:

CHIP	PORT LABEL	CARD ADDRESS(HEX)	DATA DIRECTION
U1	SGMNT	00	Output ($\overline{\text{write}}$)
U1	DCNT	01	Output ($\overline{\text{write}}$)
U1	SWTCH	02	Input ($\overline{\text{read}}$)
U1	CONT1	03(89 Initialize)	Control($\overline{\text{write}}$ only)
U2	ALAMP	04	Output ($\overline{\text{write}}$)
U2	BLAMP	05	Output ($\overline{\text{write}}$)
U2	CLAMP	06	Output ($\overline{\text{write}}$)
U2	CONT2	07(80 Initialize)	Control ($\overline{\text{write}}$ only)

II. GENERAL (con't)

The addresses on the previous page assume that the I/O line (card edge pin 78) is high (+5 Volts). In the case of a BMSC fixture, the above addresses are preceded by FF which is decoded by the BMSC as an I/O line activation.

SGMNT = FF00 Hex in software

Initialization should be accomplished in the following manner:

1) Address CONTI port

   I/O = 1
   Addr = 03
   Data= 89

2) Take the $\overline{\text{MEMW}}$ line (card edge Pin 88) low, while keeping the $\overline{\text{RST}}$, and the $\overline{\text{MEMR}}$ lines high. The conditions set up in Step 1 must be maintained while the $\overline{\text{MEMW}}$ line is low.

3) Address CON T2 port

   I/O = 1
   Addr = 07
   Data = 80

4) Repeat Step 2 using Step 3 parameters

5) The board has now been initialized to respond with the proper input/output port types. If the I/O line is low nothing on the board can ben changed or activated. The same applies for all addresses higher than 07_{hex}, even if the I/O line is high.

NOTE: See the appendix for more detailed operation of the PPI.

III. DETAILED CIRCUIT DESCRIPTIONS AND TEST SPECS

Addressing:

U1 is selected when its $\overline{\text{CS}}$ input is taken low. This is accomplished by

I/O = 1
A7, A6, A5, A4, A3, A2 = 0

The two least significant address lines A1 and A0 go directly to the chip, and are internally decoded.

U2 is selected by:

I/O = 1
A7,A6,A5,A4,A3=0
A2=1

NORTHEAST ELECTRONICS int CONCORD, NH, U.S.A		DRAWN BY	SCALE
		ENGR.	DATE
DISPLAY I/O BOARD		DRAWING NO. A-0041-13-424	REV

NEC-100R-0776

Port Descriptions:

SGMNT is initialized as an output port and is functionally split into two 4 line ports, A3-A0, and A7-A4. A3-A0 will be discussed first.

This 4 bit port is used to generate a 7 segment output from a 4 bit BCD input. U9 is a BCD-7 segment converter with active high outputs. U14 is a transistor array operating as open collector, active low LED Drivers (common anode LED). A 4 bit code at the input to U9 is converted to 7 segment as follows:

NOTE: To change the output of this port the SGMNT port must be read after the new data is written into it. This strobes the new data into U9.

U7 is preset to a code between 1 & 9, then allowed to countdown. When it reaches zero it stops counting and blanks U9. Therefore, for test purposes the clock line should be held at gnd and the A7-A4 lines should be set up for '7'. This circuit is normally used to provide the multi-brilliance capability of the 41-3A display. Normal clock frequency is 10 kHz.

SGMNT				OUTPUT PINS (CARD EDGE)							
A3	A2	A1	A0	61	62	64	63	59	60	65	
0	0	0	0	0	0	0	0	0	0	1	
0	0	0	1	1	0	0	1	1	1	1	
0	0	1	0	0	0	1	0	0	1	0	
0	0	1	1	0	0	0	0	1	1	0	
0	1	0	0	1	0	0	1	1	0	0	
0	1	0	1	0	1	0	0	1	0	0	
0	1	1	0	1	1	0	0	0	0	0	
0	1	1	1	0	0	0	1	1	1	1	
1	0	0	0	0	0	0	0	0	0	0	
1	0	0	1	0	0	0	1	1	0	0	
1	1	1	1	1	1	1	1	1	1	1	(Blank)

A '0' shall have an output voltage no greater than 3.12 Vdc at a current of 40mA per line. These lines are designed to pull the cathode of a high efficiency LED to ground. The diode anode is tied to +5 Volts.

As previously mentioned, U7 is used to control the blanking of U9. In the 41-3A system this feature controls the brightness of the Dialed Number Display. If a 100 usec clock (free running) is introduced into the card on Pin 70, U7 will countdown from the preset count (SGMNT lines A7-A4) until it reaches zero and self latches. This will blank the display until the counter is reset by reading SGMNT.

DCNT is initialized as an output port. It is essentially a pair of 4 bit ports, B7-B4, and B3-BO. The lower port will be discussed first.

The 4 bit code at B3-B0 is changed by U13 to a 1 of 16 mutually exclusive output, active low, open collector. The even outputs go directly to the card edge on the $\overline{SEL}$ lines. These lines are enable lines for the switch reading circuitry.

All outputs of U13 are used to drive the current source transistor Q1-Q15. When a transistor is turned on, its associated 'EXX' line is taken to +5 Volts. In this state the minimum voltage should be 4.5 volts DC at 400mA current. These outputs supply current to each digit in the 7 segment display under a multiplexed scheme. The following table applies to this section:

B3	B2	B1	B0	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	ACTIVE $\overline{SEL}$ LINE
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SEL 0
0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	SEL 2
0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	SEL 4
0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	
0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	SEL 6
0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	SEL 8
1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	SEL 10
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	SEL 12
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	SEL 14

The B7-B4 Section of the DCNT port is used to provide a 7 segment output and a pair of latched 3 bit outputs. In the 41-3A system, these serve as the line access display (7 segment) and the dual line selector Channel A and Channel B. Only the lower 3 bits are used since the lines are numbered from 0 to 7. The 4th bit is provided to U10 for test purposes, but under normal uses will always be 0.

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ENGR.		DATE
DISPLAY I/O BOARD	DRAWING NO. A-0041-13-424	REV

NEC-1000R-0776

The data presented to the two latch chips U11, U12 is transferred to the output by a falling transition on each chips' Pin 5. This is accomplished by making either E1 (for U11) or E9 (for U12) go from low to high. Once this transition has occurred the data inputs may change while the outputs stay the same. The following truth table will assume these transitions have occurred:

B7	B6	B5	B4	50	49	2	3	1	48	46	96	97	98	93	94	95
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	0	0	1	1	0	1	1	1	1	1	0	0	1	0	0	1
0	0	1	0	0	0	1	0	0	1	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0	0	1	1	0	1	1
0	1	0	0	1	0	0	1	1	0	0	1	0	0	1	0	0
0	1	0	1	0	1	0	0	1	0	0	1	0	1	1	0	1
0	1	1	0	1	1	0	0	0	0	0	1	1	0	1	1	0
0	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	1	1	0	0	0	0	1	0	0	1
1	0	1	0	0	0	0	1	0	0	0	0	1	0	0	1	0
1	0	1	1	0	1	0	0	0	0	0	0	1	1	0	1	1
1	1	0	0	0	1	1	0	0	0	1	1	0	0	1	0	0
1	1	0	1	1	0	0	0	0	1	0	1	0	1	1	0	1
1	1	1	0	0	1	1	0	0	0	0	1	1	0	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

SWITCH is initialized as an input port. It should NEVER be set up as an output port, as it may damage U5 or U20. It is used as an 8 bit read port, for reading most of the front panel switches in a multiplexed mode. The active state at the SB7-SB0 lines is low. The 8 bits of data at this port can be read in a complemented form at the processor data by DB7-DB0 by addressing the port and taking the MEMR line low while MEMW is high. The following will hold true, with an input 'low" to SB_X of less than .7 VDC, high greater than 3.7 VDC.

$$DB_X = \overline{SB}_X \quad \text{where X is bit 0 to 7}$$

ALAMP, BLAMP,CLAMP are identical to one another in all respects except address. Each is an output port with the card finger outputs active low. These ports are used to control the system status lamps (LEDS) in the 41-3A front panel. A '1' written to a particular bit will appear at the associated output line as a '0'. A low voltage should not exceed 1 volt at 100mA current.

Card Power Requirements:

5 volt and gnd approximately 500mA when driving display.

Voltage regulation ± 5%.

NORTHEAST ELECTRONICS int CONCORD, NH, U.S.A.	DRAWN BY	SCALE	
	ENGR.	DATE	
DISPLAY I/O BOARD	DRAWING NO. 0041-13-424		REV

NEC-100R-0776

SLEEVE HOLDING CIRCUIT MODULE

A-0041-13-433

I. APPLICABLE DRAWINGS:

B-0041-13-033 Assembly
B-0041-13-032 PC Assembly
B-0041-13-333 Schematic
9701-96641 Hole Schedule

II. SCOPE:

This document covers the operating and test specifications pertaining to the sleeve holding circuit module.

III. GENERAL:

The sleeve hold circuit is a constant current unit, where the transistor circuit operates with a constant collector current of approximately 170 mA. It may get this current from one of two sources; the -12 volt supply, or the sleeve.

If the sleeve voltage is more positive than -12 volts (approx.), then the current for the transistor is supplied by the power supply. At any sleeve voltage below -12 volts, the sleeve supplies the current.

In the case of a sleeve resistance to battery, the sleeve will be held at -12 volts, and the currents will be split between the power supply and the sleeve.

The 'gate' lead turns the circuit on for an open, and off for +5 volts.

Test Specs:

1) Apply ground to E4, -12 volts to E2, +5 volts to E3, -48 volts to E1. The sleeve current (E1) should be less than 2 mA.

2) Change E3 to open. The sleeve current should be from 150 to 200 mA.

3) Place a 1200 ohm resistance in the sleeve lead to battery. The sleeve voltage should be -12 volts, ± 2 volts.

NORTHEAST ELECTRONICS Int CONCORD, NH, U.S.A.	DRAWN BY	SCALE	
	ENGR.	DATE	
SLEEVE HOLDING CIRCUIT MODULE	DRAWING NO. A-0041-13-433		REV

NEC-100R-0776

REAR PANEL ASSEMBLY

A-0041-13-446

I. APPLICABLE DRAWINGS:

D-0041-13-046 Assembly
B-0041-13-309 AC Schematic

II. SCOPE:

This performance specification drawing pertains to the operation and setup of the power structure only, not to any other modules attached to the rear panel.

III. GENERAL:

The power structure consists of an AC section, and DC section. The AC section comprises the fan, interlock, fuses, line input, and the inputs to the two power supplies, all controlled by P39. This plug is used to provide the on/off switch function for the power unit. The DC section is comprised of the DC outputs of the two power supplies, and the DC harness P11. All measurements of voltage are made at this point, under the specified load conditions.

For AC operation, be sure that the AC Voltage Selection switch S48 is in the proper position, and that fuses of the correct value are in XF1 and XF2.

115 volt line, 115 v position, 2A fuses

230 volt line, 230 v position, 1A fuses

A power switch should be provided that breaks both sides of the line, and when closes, provides the following paths:

P39.1 to P39.4

P39.3 to P39.2

With the interlock switch (S46) in the middle, released position, turning power on at the P39 switch should cause no fan operation or DC output. If the interlock is pushed in, the fan should run, and if the interlock is pulled out all the way, the fan should run, and the interlock should maintain the out position. It would be a good idea to put a step-up transformer in the line to provide a 230 volt source, and check operation at this level also.

It may be a good idea to check continuity in the AC structure before applying line power, in which case an ohmmeter measurement from

NORTHEAST ELECTRONICS int CONCORD, NH, U.S.A.	DRAWN BY	SCALE
	ENGR.	DATE
REAR PANEL ASSEMBLY	DRAWING NO. A-0041-13-446	REV

NEC-100R-0776

ground to the two line pins in the power receptacle should exhibit very high resistance, while the center pin should be connected to chasis by less than 1 ohm.

Measurements of the DC output must be made at P11, with the following pins tied together as a common:

pins 10, 12, 13, 14, 15, 16.

There should be less than 1 ohm resistance from this common to the center pin of the AC receptacle, and chassis.

With AC power applied, and the fan running, the DC power supplies should be adjusted to the following voltages:

pin (P11)	voltage	load to ground	adjustment
4	+12 volts	12Ω, 30 watt	PSU2 'volt adj'
6	+5 volts	2Ω, 15 watt	PSU1 out 1
2	+12 volts	20Ω, 15 watt	PSU1 out 2
8	-12 volts	20Ω, 15 watt	tracks pin 2

The tolerances on the above adjustments are ±5%, and note that the ±12 volt output is tracking, with both sides adjusted by one pot. Any output should be shortable to ground, and when released, the voltage should return to normal. If the outputs are heavily loaded capacitively, the unit should be able to start from no power to full DC voltage, without having any outputs remain collapsed.

The appended data sheets apply only to the deltron power supplied originally specified for use in the 41-3A, and may not apply to any substitute supply.

OVP adjustment checks:

PSU2, OVP set for +15v ±.25 volt, pin 4.

PSU1, OVP set for ±15 v ±.25 v on dual output, pins 2 & 8.

PSU1, 5 v OVP need not be checked.

NORTHEAST ELECTRONICS inc CONCORD, NH, U.S.A.	DRAWN BY	SCALE
	ENGR.	DATE
REAR PANEL ASSEMBLY	DRAWING NO. A-0041-13-446	REV

NEC-100R-0776

LINE CONTROL MODULE

A-0041-13-448

I. APPLICABLE DRAWINGS:

B-0041-13-014 Board Assembly
B-0041-13-053 Loop/Leak Assembly
C-0041-13-314 Schematic
9700-96823 Hole Schedule

II. SCOPE:

This performance specification covers the test requirements and methods for the line control module as a complete assembly, due to the close operating characteristics of the component parts, as well as the easier test fixturing and interconnect at the module level.

III. GENERAL:

This module is the main interface and switching center between the internal 41-3A circuits, and the line to which it is attached. It contains line programming switches, a talk circuit, as well as provision for holding one line and tracing, while still testing on another. An internal reversing switch is used for those few offices which are wired backwards so that the customer doesn't have to wire special cords. A set of terminals is provided for the line meter, and the loop/leak network is accessed through this unit. All input/output to the module is through the front jacks, or the 50 pin header, J-8.

Specific Testing:

The module should first be powered up by applying a

a) ground to J8.2, and J8.4,

b) -12 volts to J8.6,

c) +5 volts to J8.3.

1) The following lines should be at +5 volts unless the corresponding button is pushed, in which case they should go to ground:

J8.50	TEST A
J8.45	TEST B
J8.43	TALK
J8.47	TRACE B
J8.49	TRACE A

NORTHEAST ELECTRONICS ntt CONCORD, NH. U S A	DRAWN BY	SCALE
	ENGR.	DATE
LINE CONTROL MODULE	DRAWING NO. A-0041-13-448	REV

NEC-100R-0776

2) There should always be continuity according to the following table, regardless of which button is pushed.

from J8 pin	Line Jack Label	to Jack reference
15	cha A tip	J14
17	cha A ring	J14
25	cha A sleeve	J14
19	cha B tip	J15
21	cha B ring	J15
23	cha B sleeve	J15
9	bridge tip	J16
7	bridge ring	J16
5	bridge sleeve	J16
2	talk tip (rt)	J13

3) J8.2 to J8.27 should measure open, unless a plug is inserted into either the Test A or Test B jacks, at which time J8.27 should then be shorted to J8.2, ground.

4) With the t-r reversing switch, S7, in the forward, T+ NORM position, and the EXT switch in the out position, the following continuities should exist:

from J8.9	bridge tip	to	J8.31
from J8.7	bridge ring	to	J8.33

If the reversing switch is moved to the rear position, the following should have continuity:

from J8.9	bridge tip	to	J8.33
from J8.7	bridge ring	to	J8.31

5) Put the switch back to the forward position, for tip normally positive. If a voltage of, say, 5 volts is placed across the bridge jack, with tip positive, ring negative then the quick disconnect on the board labelled 21 should be positive with respect to the QD labelled 22. These are the meter attachment points.

6) With the EXT switch out, and the line reverse switch forward, the following must be continuity tested and true:

bridge tip	to	J8.31
bridge ring	to	J8.33
bridge sleeve	to	J8.1

With the EXT switch depressed, and the line reverse switch forward, the following must have continuity:

bridge tip	to	external tip
bridge ring	to	external ring
bridge sleeve	to	external sleeve

J8.1 must not conduct to anything.

7) If a 52-A headset is plugged into the talk jacks, and a scope or voltmeter is attached to the bridge tip/ring, when the TALK button is pushed, and the headset talked into, a signal should appear at the bridge jack.

8) An AC signal, 1004 hz, 0 dbm (900 ohm) should be applied from J8.11 to J8.13. If the TRACE A button is pushed, the following must occur:

a. A DC resistance of 900 ohm ±10% must appear from Chan A tip to Chan A ring.

b. The 1 khz signal should be observed across channel A tip/ring.

c. Releasing the button should remove both the ac signal, and the resistor.

9) This will be the same as the above step, except channel B should be used. Tracing on one channel should not be seen on the other except as low level crosstalk, more than 30 dB down, terminated 900 ohms.

When either trace switch is pushed, the corresponding sleeve must show a ground conduction.

10) Loop resistance may be seen by placing an ohmmeter across J8.35 and U8.36. The NORMal resistance should be a short circuit, with clockwise switch rotation giving the following resistances, ±5%:

600, 800, 1000, 1100, 1200, 1300, 1400, 1500, 1600, 1800, 1900 ohms.

NORTHEAST ELECTRONICS inc CONCORD, NH, U.S.A.	DRAWN BY	SCALE	
	ENGR.	DATE	
LINE CONTROL MODULE	DRAWING NO. A-0041-13-448		REV

NEC-100R-0776

11) Leak values are more difficult to test, and are given in two groups, AC testing, and DC testing.

Normal leak should exhibit an open circuit.

AC testing should be done at a frequency of 1000 hz, measuring the following approximate AC impedances by a classic half-voltage method, not a bridge (GR Impedance).

Leak A	3,397 ohms
Leak B	10,200 ohms
Leak C	631 ohms
Leak D	651 ohms

The above values are calculated with the nominal values of the leak components in mind. Leak C and D may be difficult to distinguish from each other due to their closeness, and component tolerance, however, Leak D should always have a higher impedance than Leak C.

The next four values are DC resistances, and should be measured as follows:

7.15	position	7.15K ±2%
7.5	position	7.50K ±2%
10.0	position	10K ±2%
15	position	15K ±2%

NORTHEAST ELECTRONICS inc CONCORD, NH, U.S.A.	DRAWN BY	SCALE
	ENGR.	DATE
LINE CONTROL MODULE	DRAWING NO. A0041-13-448	REV

MCS MODULE

A-0041-13-449

I. APPLICABLE DRAWINGS:

D-0041-13-049 Module Assembly
B-0041-13-016 Board Assembly
D-0041-13-316 Schematic

II. SCOPE:

This performance spec. covers the MCS module test requirements and methods. The testing is done at the completed module level instead of the pc board level due to easier interconnect.

III. GENERAL:

The MCS module consists of two 8-line selectors, channel A and channel B, as well as 16 310-type jacks for tip-ring-sleeve access from the office side. All input/output to the module is either via the 310 jacks, or the 16 pin socket J-10.

The module contains a ground relay that removes the ground from the sleeve contacts when the module is not powered-up. This is to keep a ground from going out, and holding up an office, if the unit is connected, but not plugged in. Each jack automatically has a ground applied to the sleeve if there is not a plug in that jack. The ground is removed when a plug is inserted.

Channel selection is controlled by 3 lines/channel at J-10, with the active state of the line low. For any line selected, there should be continuity between the selected jack, and the channel T,R,S lines at J-10. There should be no tip-ring reversals in the MCS unit, and only one jack per channel may be selected at one time. There should be no connection between the two channels.

It would be wise to look at the underside of the PC board, and be sure that it is not shorting to any of the top row of jacks. If it is shorting, it probably means that the jackblock has been installed wrong side up.

The following table gives the proper line selection coding. Note that the unit receives ground and +12 volts thru J-10, and the relay select lines that are inactive should be up at this voltage (1 = +12v, 0 = GND).

NORTHEAST ELECTRONICS int CONCORD, NH, U.S.A.		DRAWN BY	SCALE
		ENGR.	DATE
MCS MODULE		DRAWING NO. A-0041-13-449	REV

NEC-100R-0776

Channel A

A.C	A.B	A.A	Jack selected	Line
1	1	1	J18	0
1	1	0	J19	1
1	0	1	J20	2
1	0	0	J21	3
0	1	1	J22	4
0	1	0	J23	5
0	0	1	J24	6
0	0	0	J25	7

CHANNEL B

B.C	B.B	B.A		
1	1	1	J26	0
1	1	0	J27	1
1	0	1	J28	2
1	0	0	J29	3
0	1	1	J30	4
0	1	0	J31	5
0	0	1	J32	6
0	0	0	J33	7

Maximum current is drawn from the +12 volt supply with both channels at 7, and should be approximately 750 mA.

41-3A TTY INTERFACE

C-0041-13-464

APPLICABLE DRAWINGS:

C0041-13-364	Schematic
B0041-13-064	Assembly
9700-96963	Hole Schedule

SCOPE:

This document pertains to the operation and testing of the 41-3A TTY interface board only.

GENERAL:

This board provides the parallel/serial and serial/parallel conversions for communication between a 41-3A and external serial ASCII devices. The parallel interface is comparible with the Northeast Electronics BMSC Bus structure, while the serial interface ports are 20 ma current loop, and EIA RS232-C.

The circuits consist of two essentially identical channels, one to be labeled "TTY", the other "AUX."

Each channel consists of an 8251 Programmable Communications Interface (PCI), and current loop, EIA to TTL converters. A dual baud rate generator (U3) provides clock signals to each channel independently.

The PCI provides serial parallel conversion, allowing the processor to read and write 8 bit Hex ASCII words to the PCI. The PCI, along with the baud rate generator converts the parallel data to the proper serial ASCII format, at the desired speed.

The current loop receiver is an voltage threshold system, requiring a contact closure at J35 Pins 9,20(Aux)&9,13(Remote), or a sufficiently negative value at Pins 19 or 20 to cause 20 ma current flow. This is the "mark" status.

Also on the board are two PROMS's containing the option software, accessible from the CPU Bus.

NORTHEAST ELECTRONICS Int CONCORD, NH, U.S.A.		DRAWN BY S. Nilson	SCALE
		ENGR. GKN	DATE 1-9-79
NEC-100R-0776	41-3A TTY INTERFACE	DRAWING NO. 0041-13-464	REV /

The EIA Receivers require a bipolar, ground referenced signal of $\pm$ 3 volts minimum swing. The (-) voltage is the "marking" condition.

The EIA transmitter (J35 Pin7) provides a bipolar signal of $\pm$ 5 volts minimum into 3000 ohm. The marking condition is (-) voltage. Maximum signal swing is $\pm$ 12 volts.

The current loop transmitter can operate as either a current source (active) or transistor switch (passive). The mode is strap selectable.

ACTIVE MODE

STRAP A to X, B to Y, C to Z.

A current of 23 ma $\pm$ 5 will flow through a short circuit between J35 Pins 2 and 5 in the "marking" condition. A "Space" will cause currrent to drop to less than 1 ma.

PASSIVE MODE

STRAP A to Y, B to Z, C to C'.

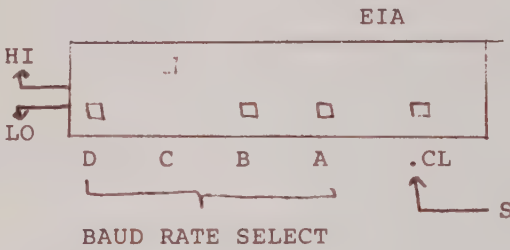
Pins 2 & 5 on J35 will appear as a contact closure ($\geq$ 8V drop) for an externally supplied current. Pin 2 must be (+) W/R to Pin 5. The closure is provided during the mark condition. The space will provide $\geq$ 100 K ohm of resistance for a measurement voltage $<$ 15 volts D.C.

The Remote and Aux. channels have seperate programming switches. The Aux. channel uses 4 bits to get the receiver baud rate, and 1 bit to choose EIA or CL input mode. The remote channel uses 4 bits for baud rate, 3 bits for parity control, and 1 bit for CL-EIA selection. If the EIA inputs are used, the respective CL inputs must be open.

NORTHEAST ELECTRONICS int CONCORD, NH, U.S.A	DRAWN BY S. Nilson	SCALE --	
	ENGR. SFN	DATE 1-9-79	
41-3A TTY INTERFACE	DRAWING NO. 0041-13-464	REV /	

NEC-100R-0776

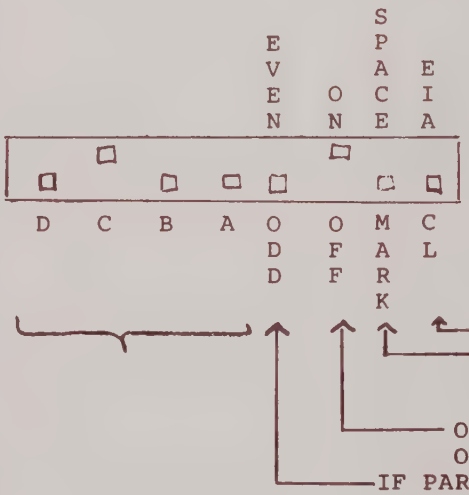
Page 4



AUX CHANNEL

D	C	B	A	BAUD	U13.7 FREQ.	D	C	B	A	BAUD	U13.7 FREQ.
L	L	L	L	50	.8 KHz	H	L	L	L	1800	28.8
L	L	L	H	75	1.2	H	L	L	H	2000	32.081
L	L	H	L	110	1.76	H	L	H	L	2400	38.4
L	L	H	H	134.5	2.1523	H	L	H	H	3600	57.6
L	H	L	L	150	2.4	H	H	L	L	4800	76.8
L	H	L	H	300	4.8	H	H	L	H	7200	115.2
L	H	H	L	600	9.6	H	H	H	L	9600	153.6
L	H	H	H	1200	19.2	H	H	H	H	19,200	316.8

REMOTE CHANNEL



D	C	B	A	BAUD	U3.3 FREQ,KHZ	D	C	B	A	BAUD	U3.3 FREQ.. KHZ
L	L	L	L	50	.8	H	L	L	L	1800	28.8
L	L	L	L	75	1.2	H	L	L	H	2000	32.081
L	L	H	H	110	1.76	H	L	H	L	2400	38.4
L	L	H	H	134.5	2.1523	H	L	H	H	3600	57.6
L	H	L	L	150	2.4	H	H	L	L	4800	76.8
L	H	L	L	300	4.8	H	H	L	H	7200	115.2
L	H	H	H	600	9.6	H	H	H	L	9600	153.6
L	H	H	H	1200	19.2	H	H	H	H	19,200	316.8

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41-3A TTY OPTION | DRAWING NO. 0041-13-464 | REV /

NEC-100R-0776

ADDRESSING:

F000 - F3FF	U5 PROM
F400 - F7FF	U6 PROM
FFF0	AUX. DATA, U1
FFF1	AUX. CONTROL REG, U1
FFF2	REMOTE DATA, U2
FFF3	REMOTE CONTROL REG. , U2
FFF4	REMOTE SWITCH PORT S1, U14, U15

INTIALIZATION:

1. Power up card
2. Reset card by taking $\overline{\text{RESET}}$ to GND, then to +5 volts
3. Address U1 control
4. Write 4AH to U1 control
5. Write 37H to U1 control
   Aux. port now set for 7 data bits, one stop bit
6. Address U2 control
7. Write 6EH to U2 control (for 1 stop bit) or
   EEH to U2 control (for 2 stop bits)
8. Write 37H to U2 control
   Remote port now set for 8 bit data, 1 to 2 stop bits,
   Xmit & Rec. enabled.
9. Card is now ready to use.

*NOTE: All parity control is software determined, and these switches are only read by the CPU.

NORTHEAST ELECTRONICS inc CONCORD, NH, U.S.A.	DRAWN BY S. Nilson	SCALE ---
	ENGR. SLN	DATE 1-9-79
41-3A TTY INTERFACE	DRAWING NO. 0041-13-464	REV /

NEC-100R-0776

BUS INTERFACE OPERATIONS:

After the PCI's have been initialized, they may be written to and read from according to the following rules:

1) Read Data from Serial Input:

If data has been received, the 2^1 bit (02 HEX) in the control register will be set. This bit may be read by the testing processor. If the bit is set, the data may be read from the data resistor. This operation automatically clears the bit in the control register, making it ready to accept the next serial character.

2) Write Data to Serial Output:

To write data, the transmitter buffer must be empty. This is checked by reading the control register, and looking at the 2^3 bit (04H). If the bit is set to "1", the buffer is ready. The 8 bit word may then be written to the data port. This control bit will be reset until the serial ASCII character has been transmitted.

CARD EDGE SIGNALS:

1) All inouts standard TTL Levels.
2) Ø2 required - derived from BMSC.
3) Power Pins

Pin 2	+ 5V ± 5% < 200mA.
Pin A	+12V ± 5% < 190mA.
Pin C	-12V ± 5%, 35mA ± 20mA.
Pin 1	Ground
Pin B	- 5V ± 5%, < 90mA.

J35 SIGNALS

PIN	
1	EIA input from Aux. channel
20	+CL input from Aux. channel ≈ 4K Zin
9	-12 Volts thru 500 ohm, -CL input form Aux. channel
4	GND
15	+12 volts thru 470 ohm
19	+CL input from remote channel ≈ 4K Zin
13	-CL input from remote channel -12V thru 500 ohm
3	EIA input from remote channel
7	EIA output to remote channel
2 & 5	CL output to remote channel

NORTHEAST ELECTRONICS int
CONCORD, NH, U.S.A.

DRAWN BY S. Nilson SCALE --
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